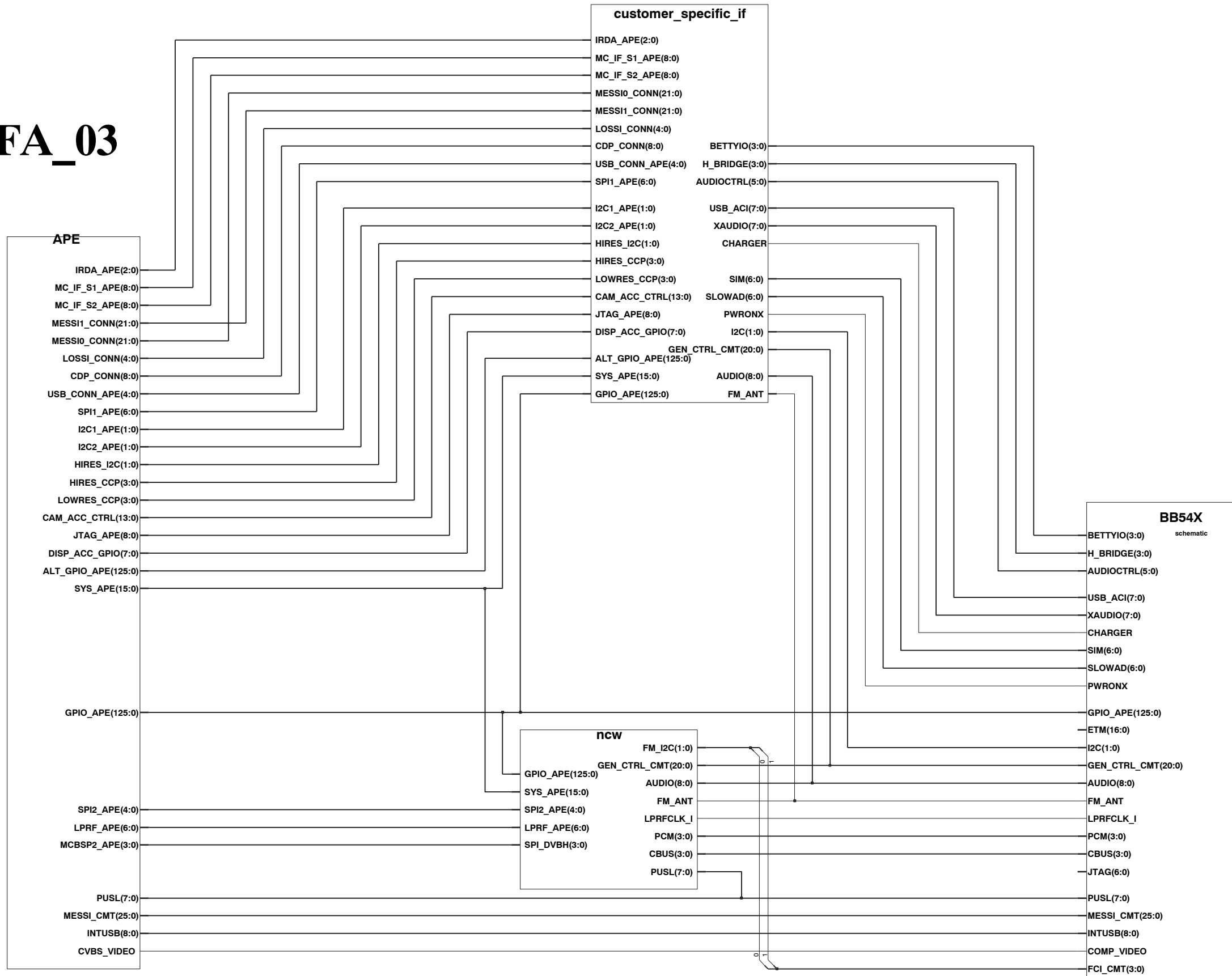
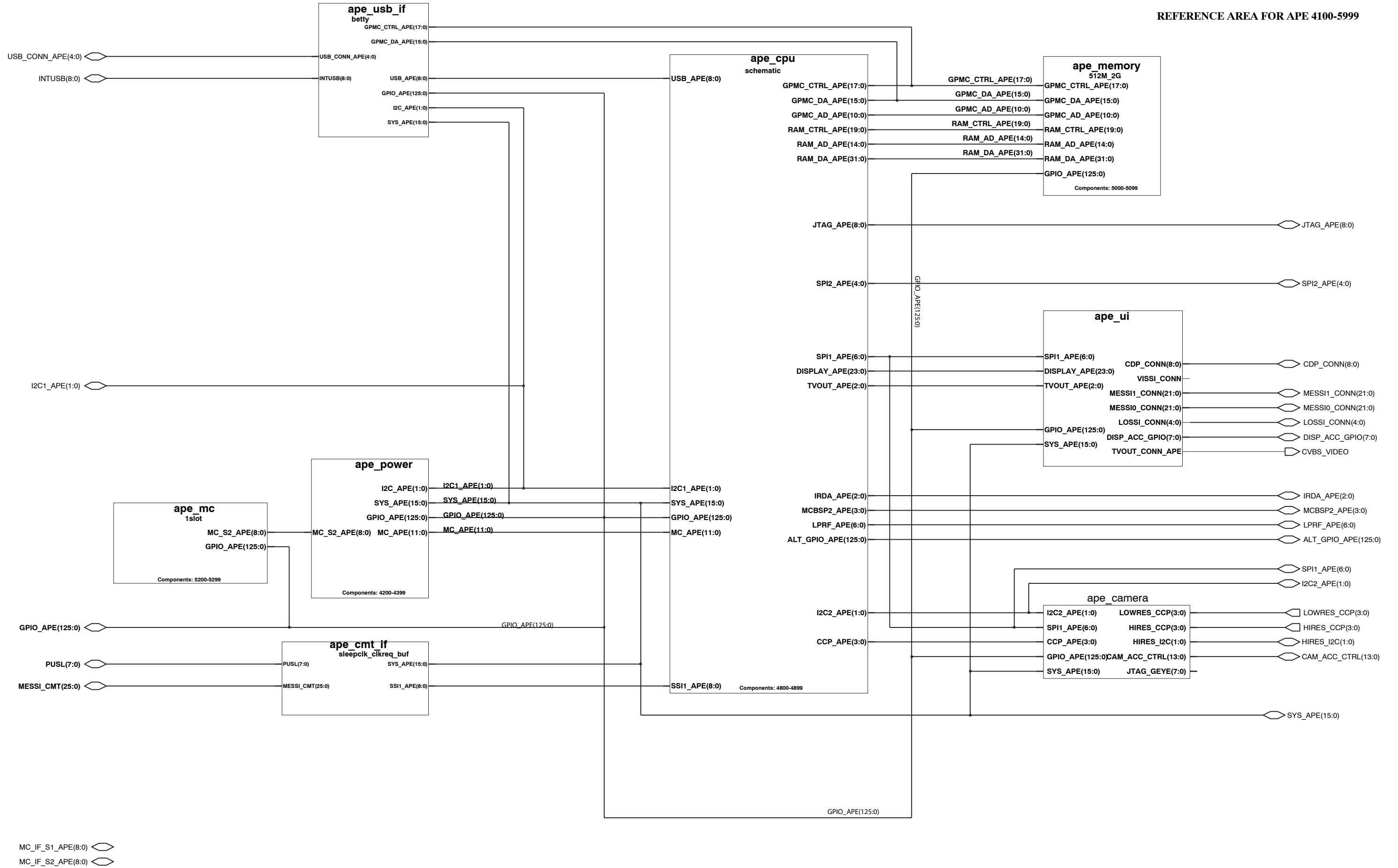


2FA_03



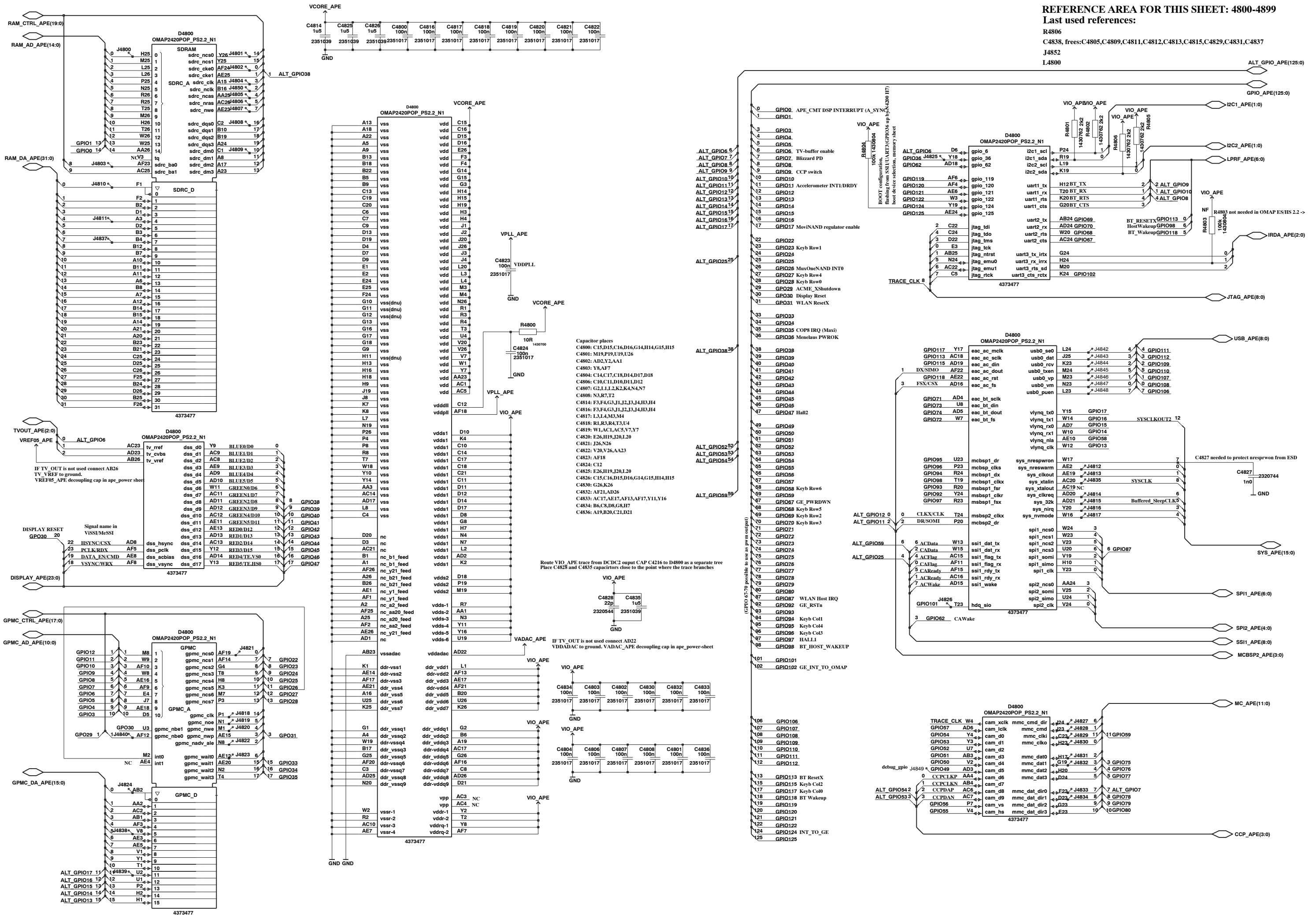
REFERENCE AREA FOR APE 4100-5999



REFERENCE AREA FOR THIS SHEET: 4800-4899

Last used references:

- R4806
- C4838, fuses: C4805, C4809, C4811, C4812, C4813, C4815, C4829, C4831, C4837
- J4852
- L4800



Last used references:

D5000

R5004, frees: R5000

GPMC_AD_APE(10:0)

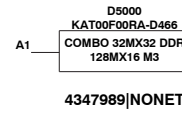
RAM_AD_APE(14:0)

RAM_CTRL_APE(19:0)

GPMC_CTRL_APE(17:0)

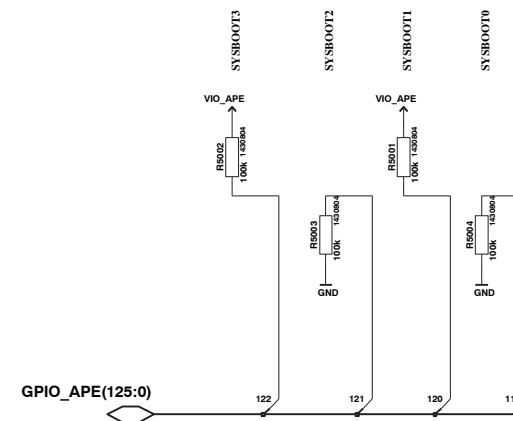
GPMC_DA_APE(15:0)

RAM_DA_APE(31:0)



POP3 Memory Stacked on top of D4800 OMAP2420POP
NONET Geometry for partlists

1G/2G memory code

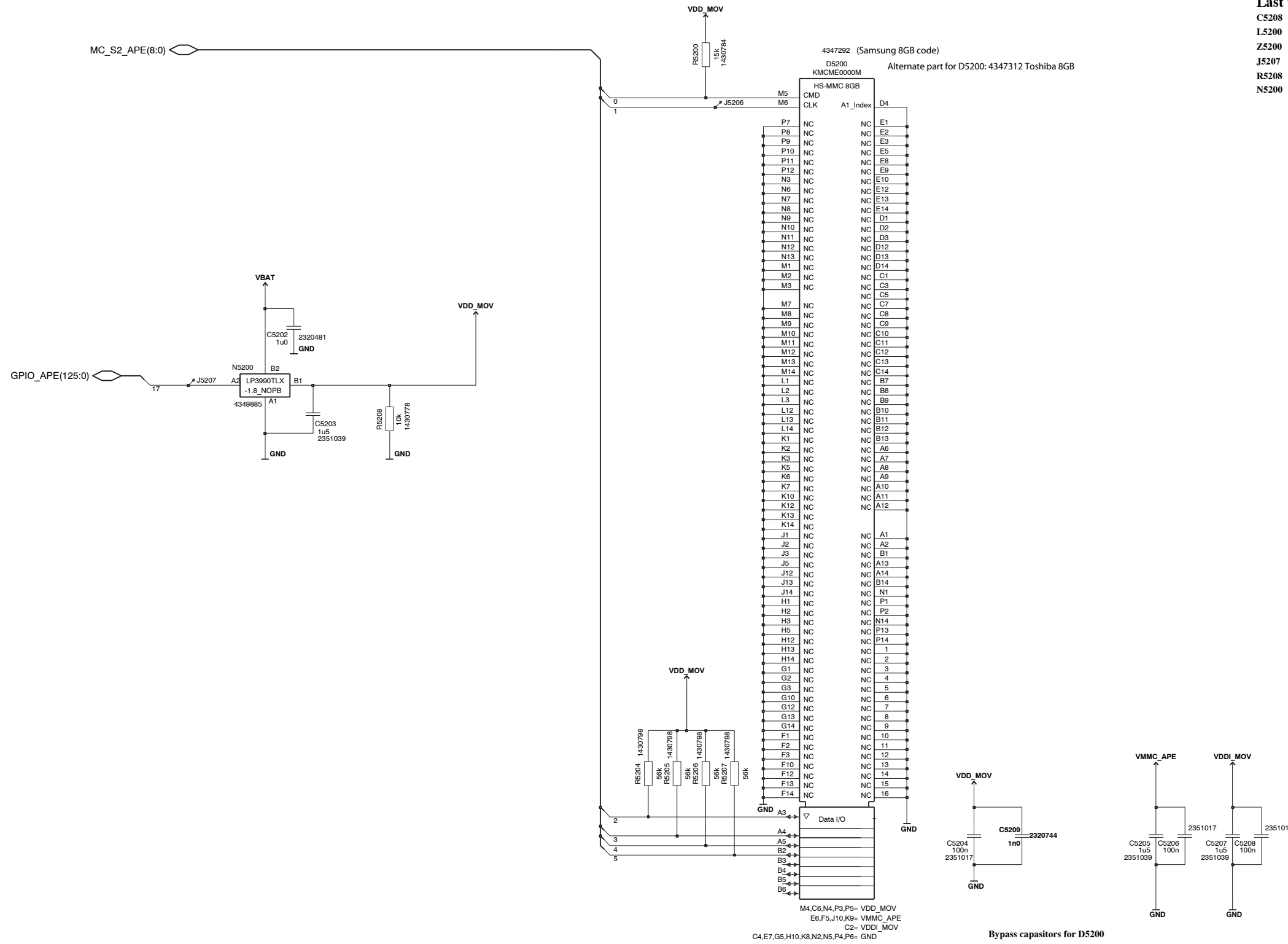








BOOT configuration,
1010=boot from 16-bit MuxedOneNAND

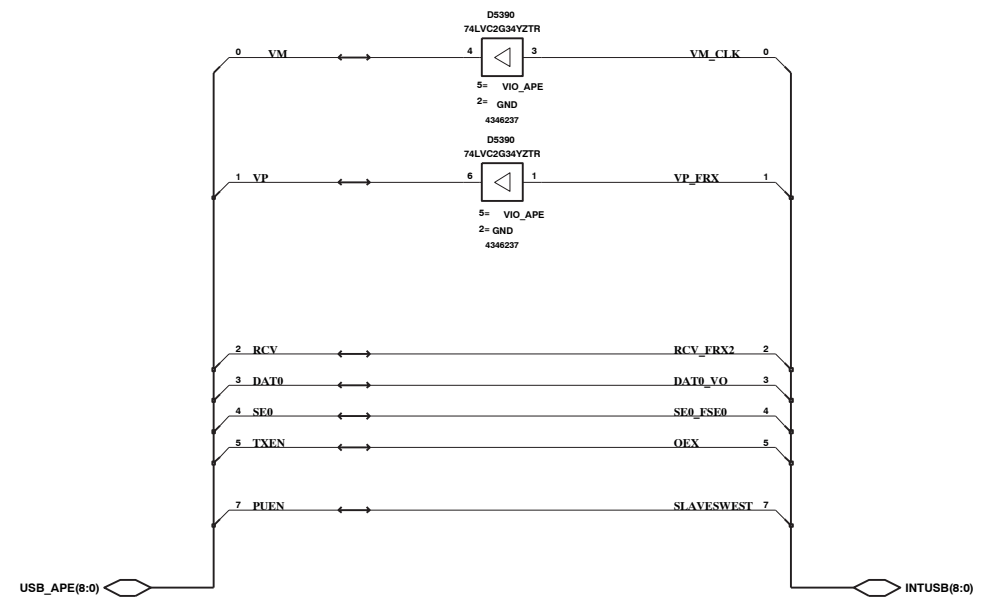
REFERENCE AREA FOR THIS SHEET: 5200-5249

Last used references:

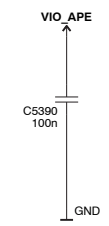
- C5208
- L5200
- Z5200
- J5207
- R5208
- N5200

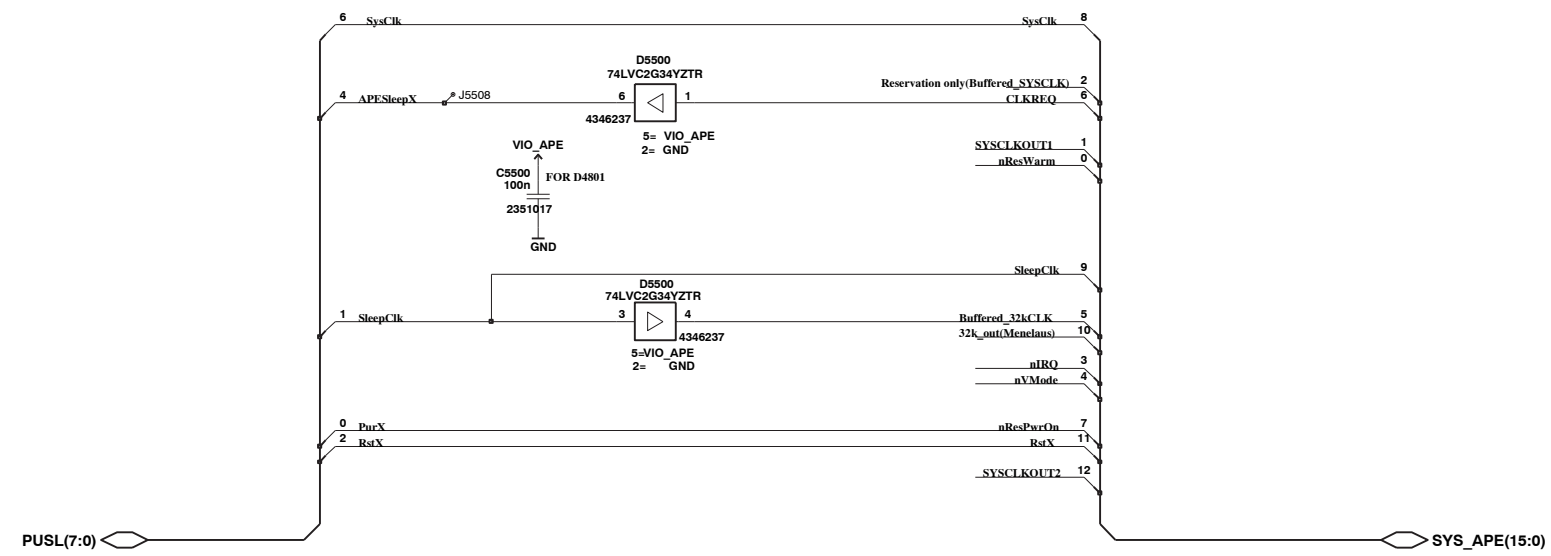
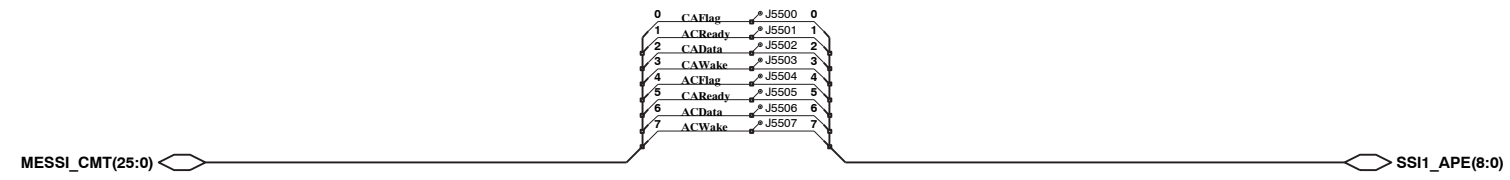


- SYS_APE(15:0) 
- GPMC_CTRL_APE(17:0) 
- GPIO_APE(125:0) 
- GPMC_DA_APE(15:0) 
- I2C_APE(1:0) 
- USB_CONN_APE(4:0) 

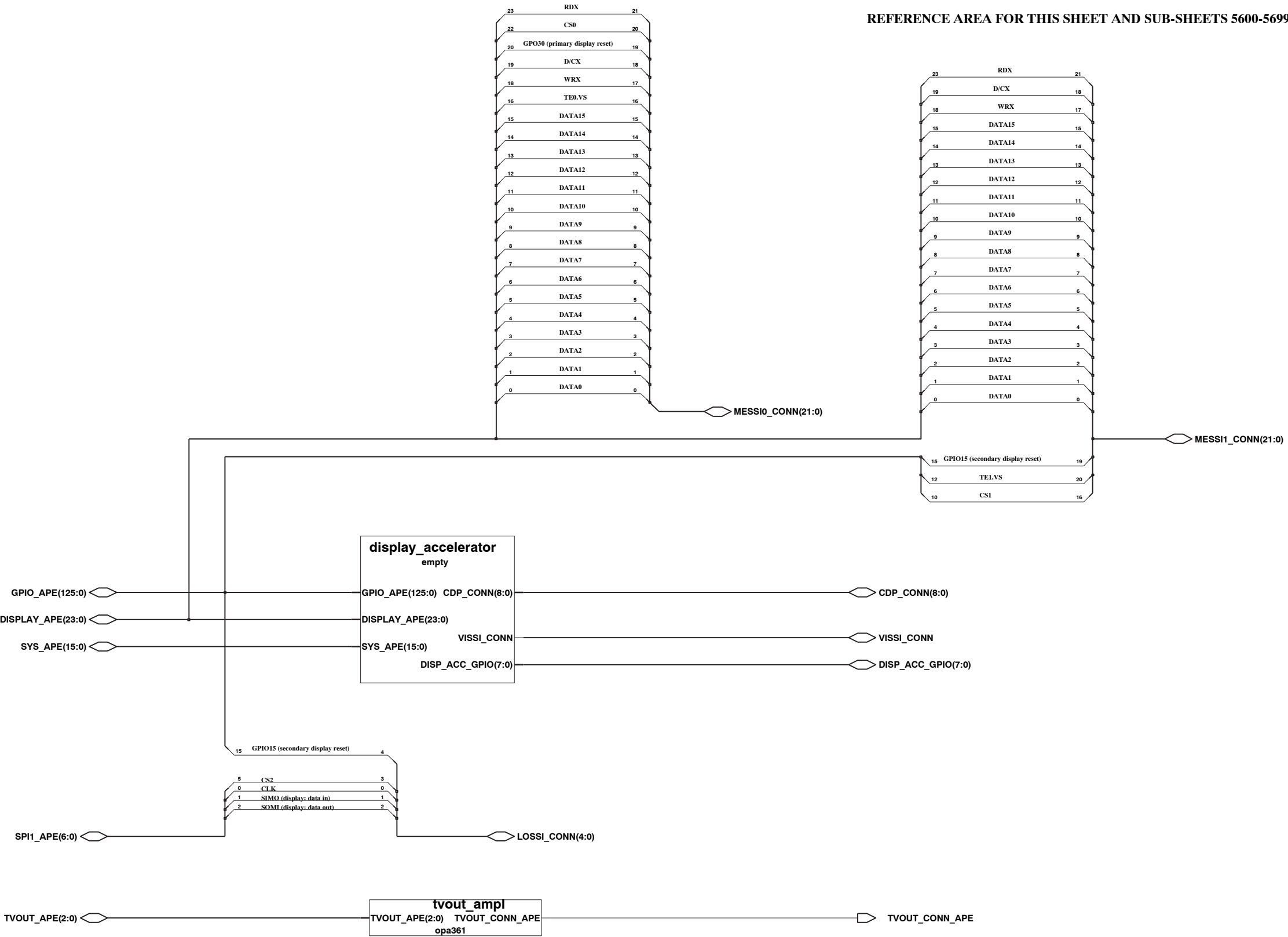


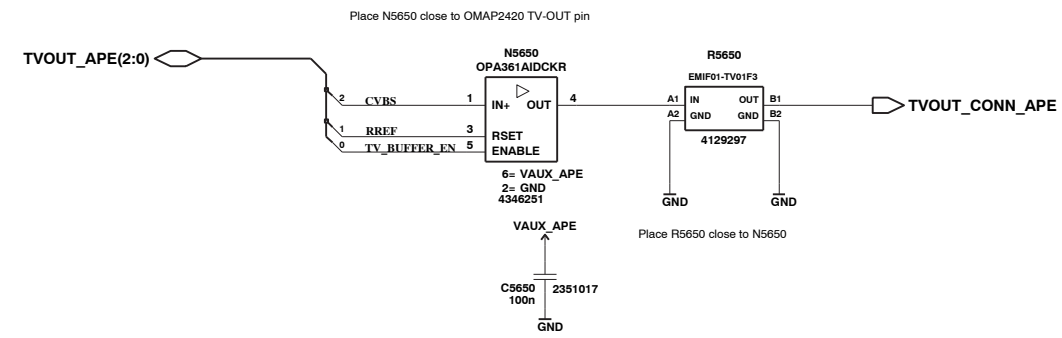
Bypass capacitor for D5390

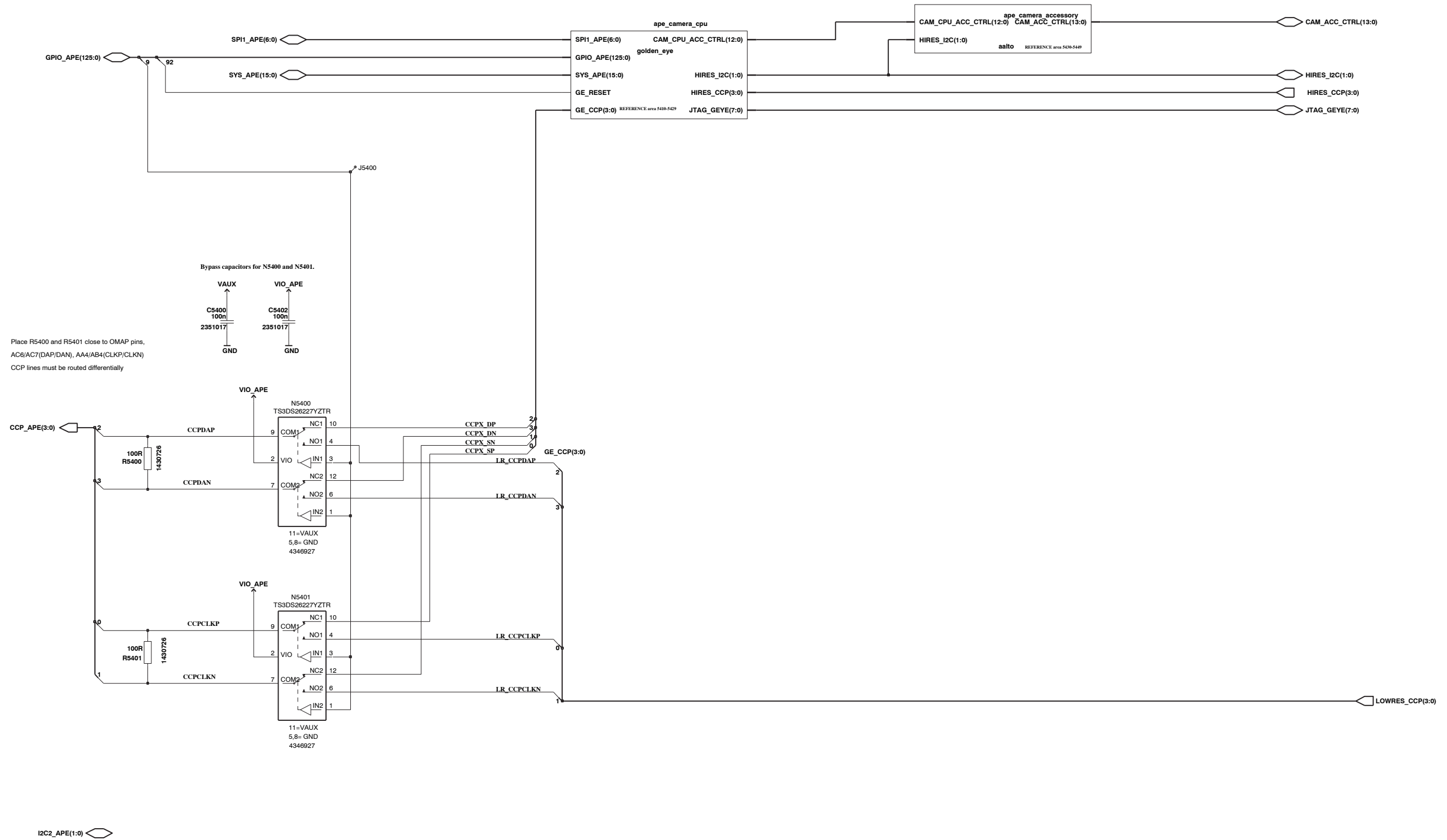




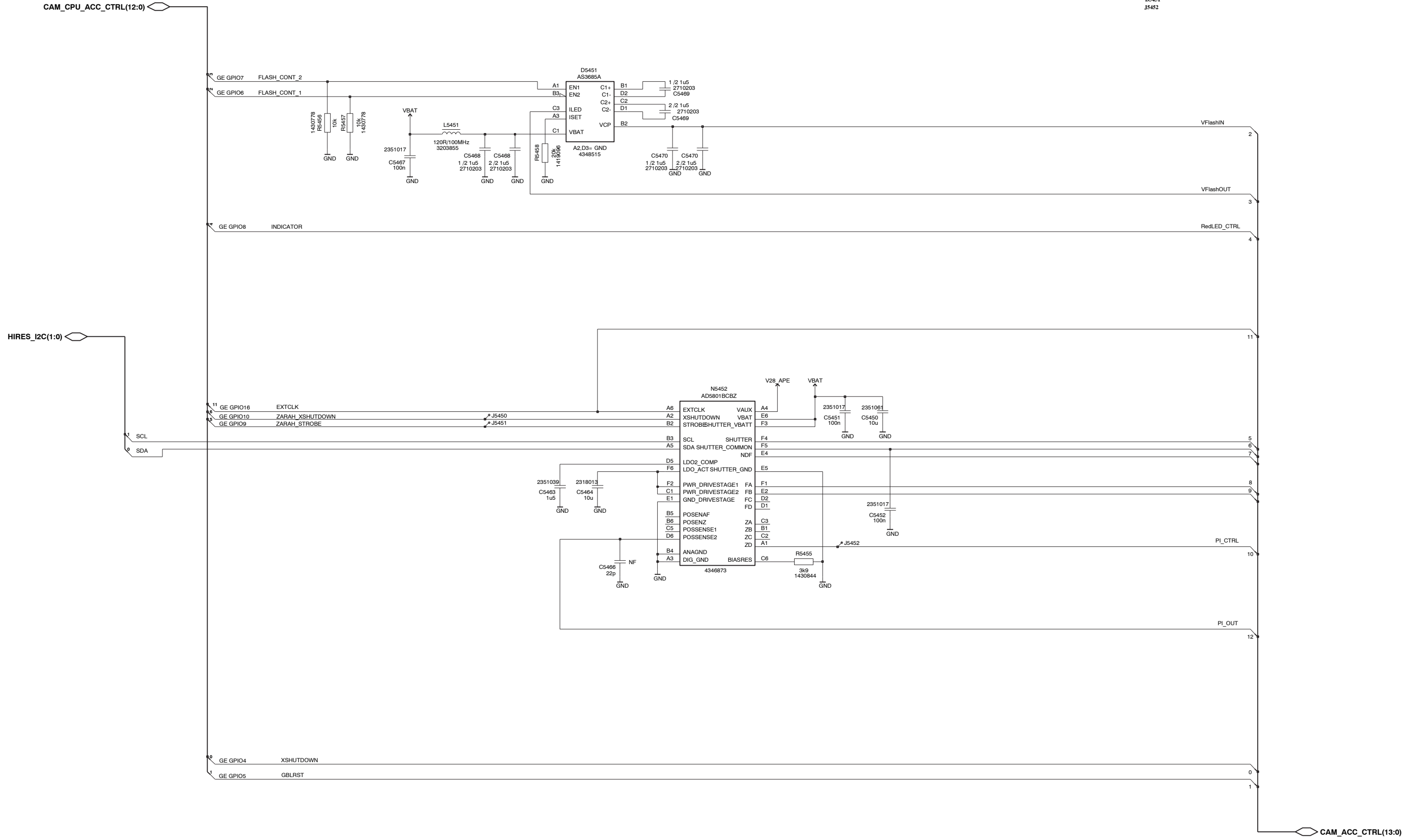
REFERENCE AREA FOR THIS SHEET AND SUB-SHEETS 5600-5699





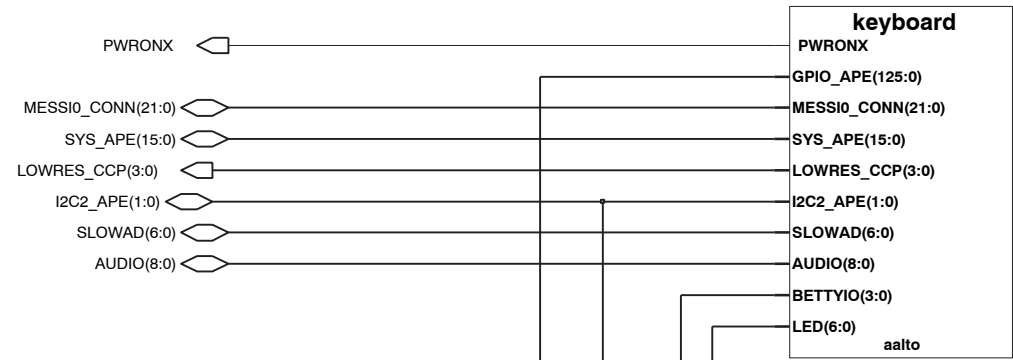


Last used references:
 C5470
 R5458
 L5451
 D5451
 J5452



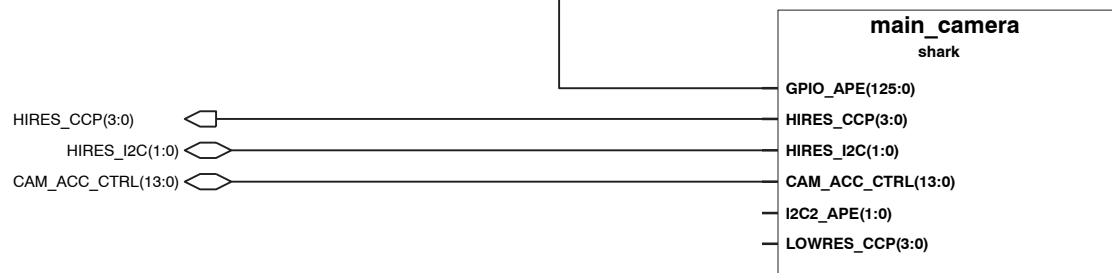
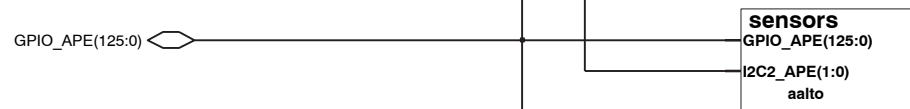
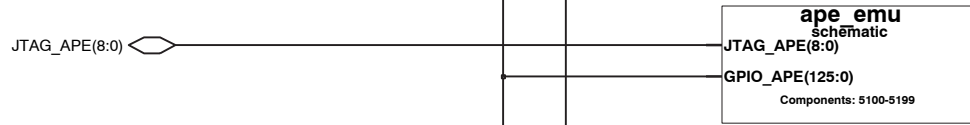
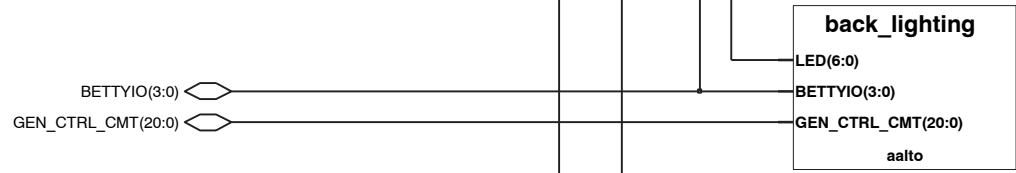


- XAUDIO(7:0)
- USB_ACI(7:0)
- CHARGER
- AUDIOCTRL(5:0)
- H_BRIDGE(3:0)



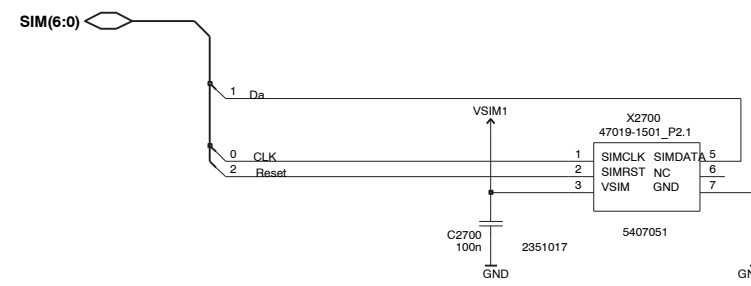
- I2C(1:0)

FM_ANT



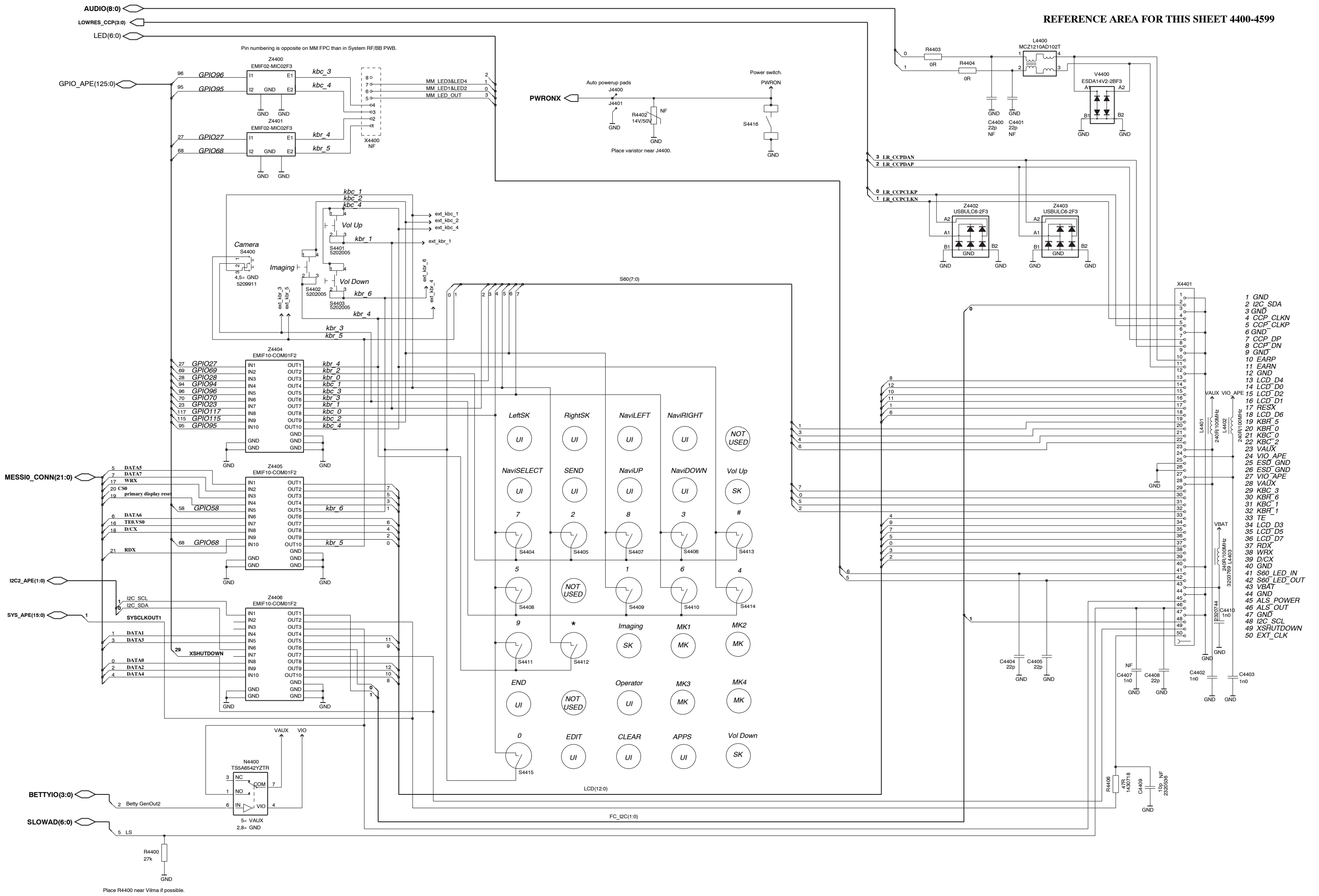
- LOSSI_CONN(4:0)
- MESSI1_CONN(21:0)
- I2C1_APE(1:0)
- CDP_CONN(8:0)
- SPI1_APE(6:0)
- USB_CONN_APE(4:0)
- ALT_GPIO_APE(125:0)
- DISP_ACC_GPIO(7:0)

Last used references
X5250



MC_IF_S1_APE(8:0)

MC_IF_S2_APE(8:0)



Pin numbering is opposite on MM FPC than in System RF/BB PWB.

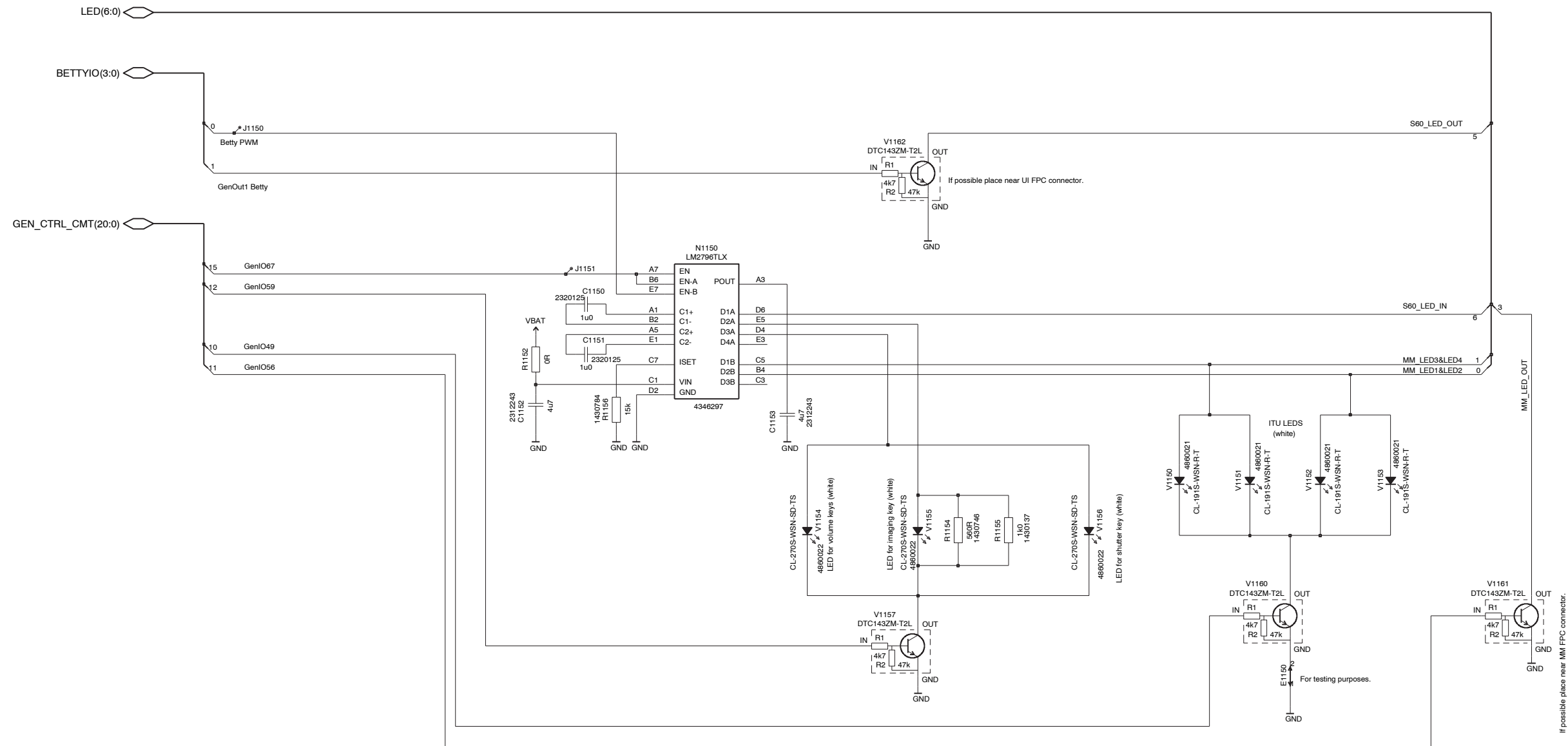
Place varistor near J4400.

Place R4400 near Vilma if possible.

- 1 GND
- 2 I2C SDA
- 3 GND
- 4 CCP CLK
- 5 CCP CLK
- 6 GND
- 7 CCP DP
- 8 CCP DN
- 9 GND
- 10 EARP
- 11 EARN
- 12 GND
- 13 LCD_D4
- 14 LCD_D0
- 15 LCD_D2
- 16 LCD_D1
- 17 RESX
- 18 LCD_D6
- 19 KBF_5
- 20 KBF_0
- 21 KBC_0
- 22 KBC_2
- 23 VAUX
- 24 VIO_APE
- 25 ESD_GND
- 26 ESD_GND
- 27 VIO_APE
- 28 VAUX
- 29 KBC_3
- 30 KBF_6
- 31 KBC_1
- 32 KBF_1
- 33 TE
- 34 LCD_D3
- 35 LCD_D5
- 36 LCD_D7
- 37 RDX
- 38 WRX
- 39 D/CX
- 40 GND
- 41 S60_LED_IN
- 42 S60_LED_OUT
- 43 VBAT
- 44 GND
- 45 ALS_POWER
- 46 ALS_OUT
- 47 GND
- 48 I2C_SCL
- 49 XSRUTDOWN
- 50 EXT_CLK

REFERENCE AREA FOR THIS SHEET 1150-1199

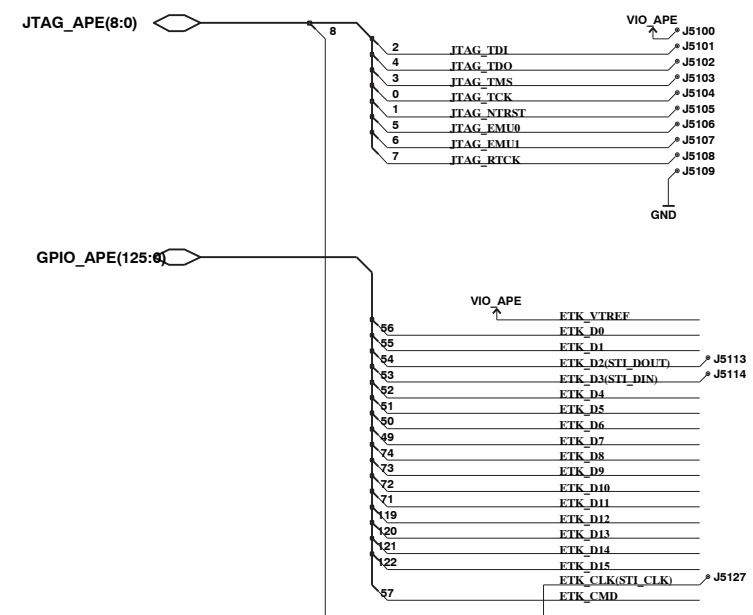
Last used references
R1156

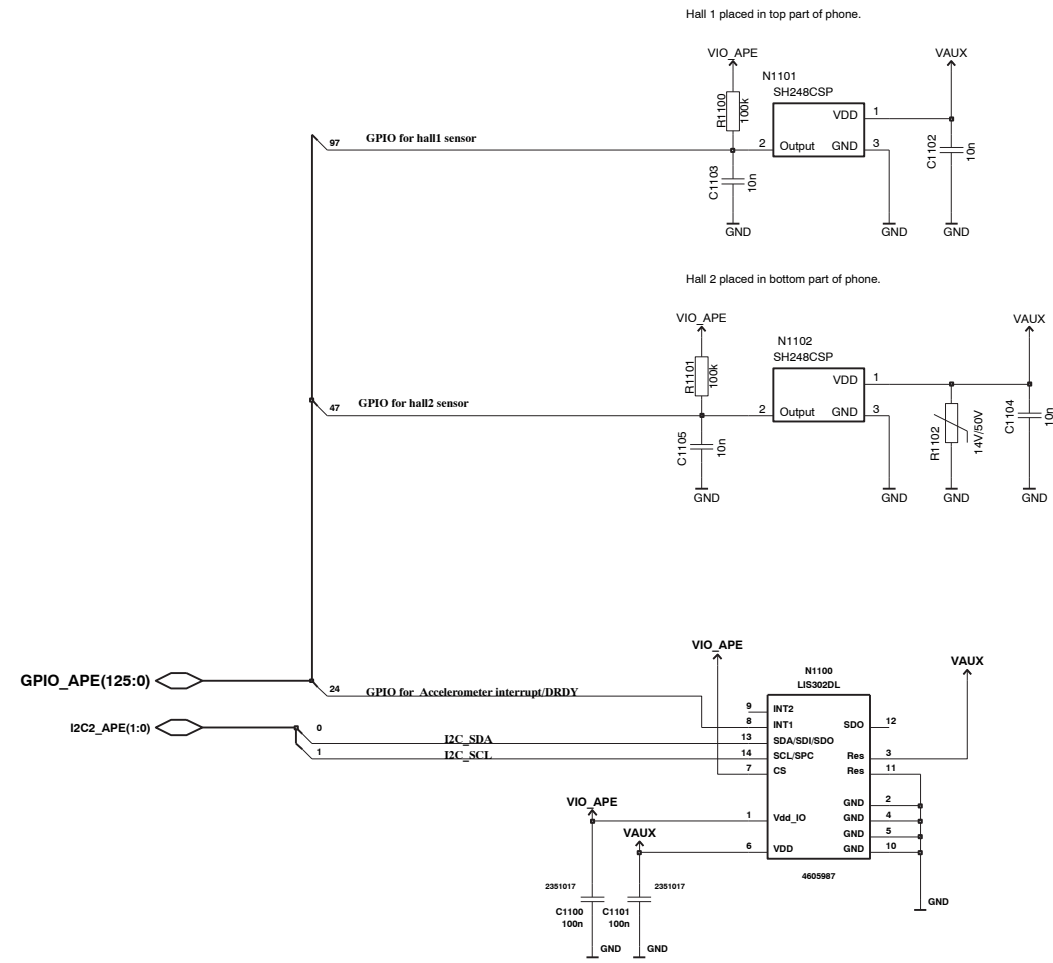


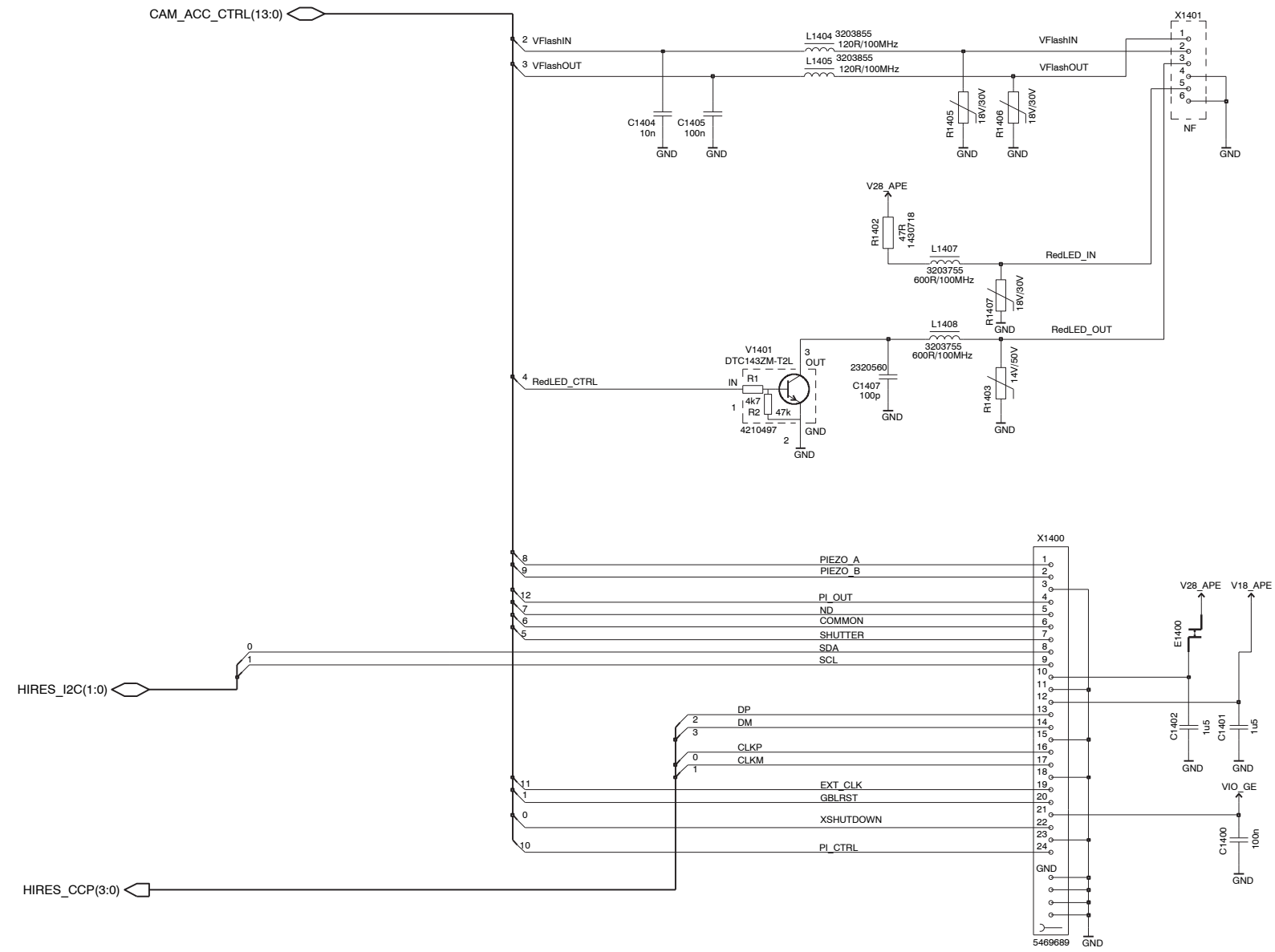
REFERENCE AREA FOR THIS SHEET: 5100-5199

Last used references:


J5129

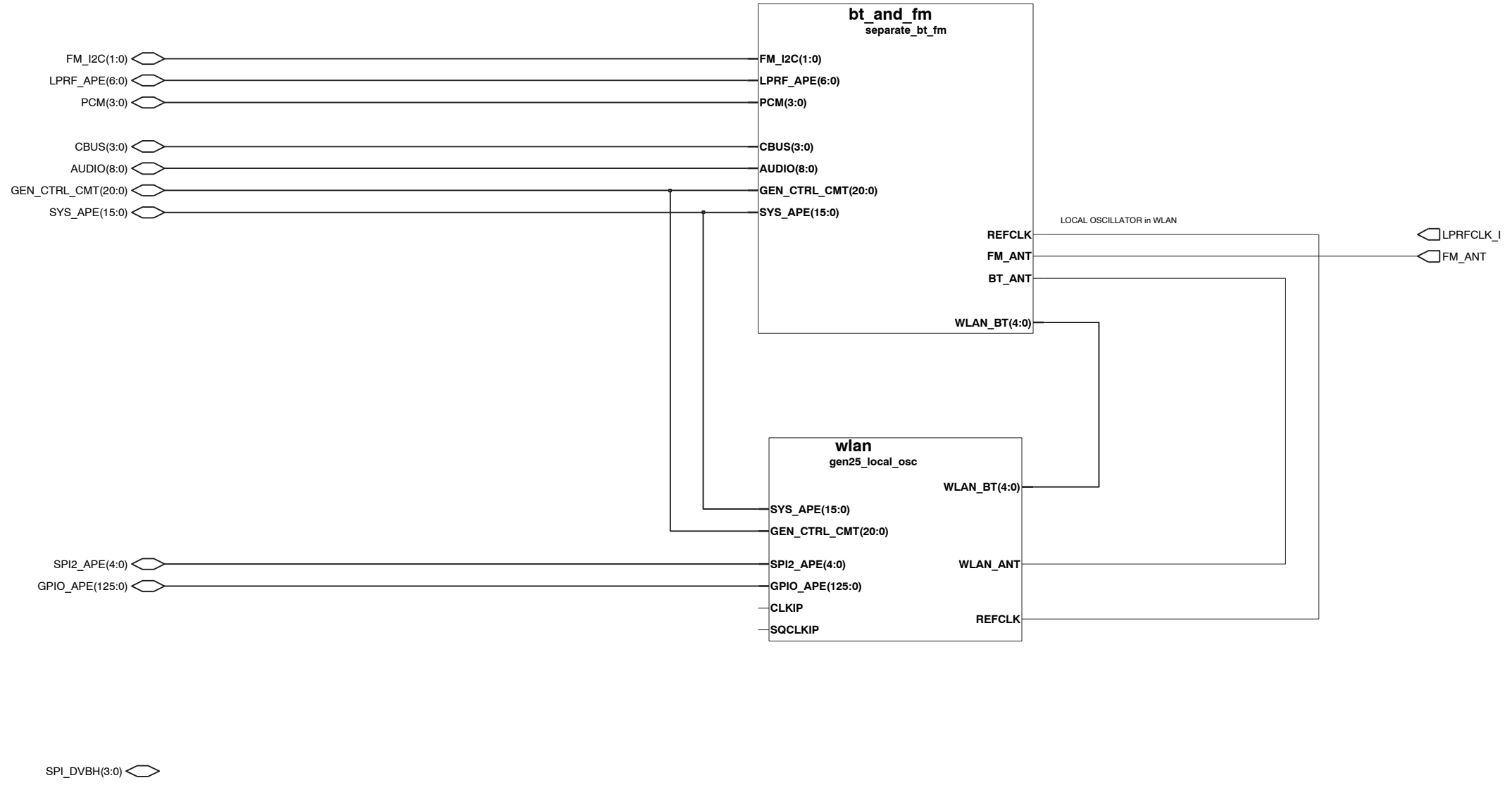





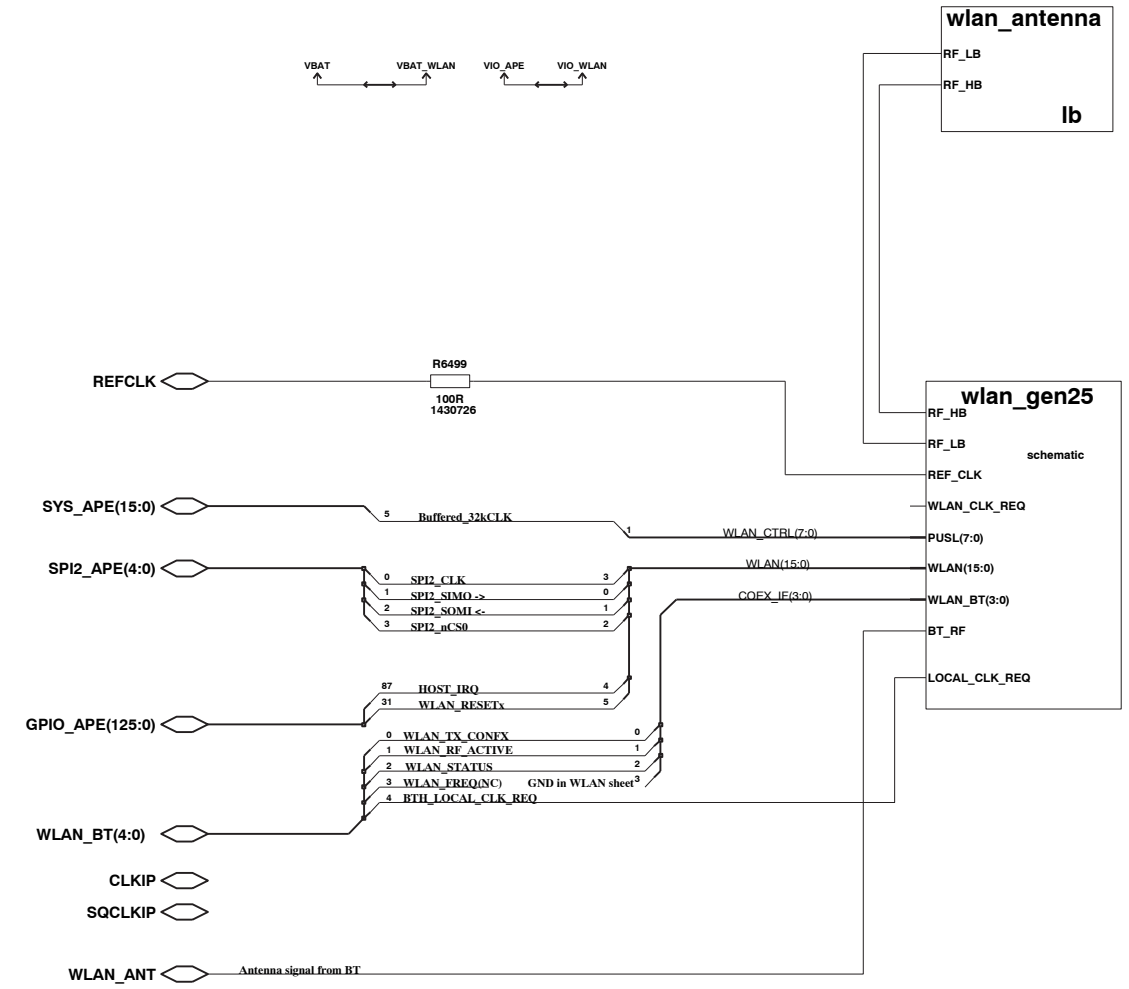


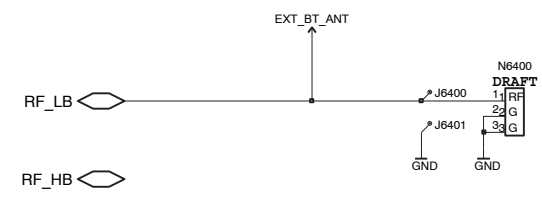
- GPIO_APE(125:0)
- I2C2_APE(1:0)
- LOWRES_CCP(3:0)

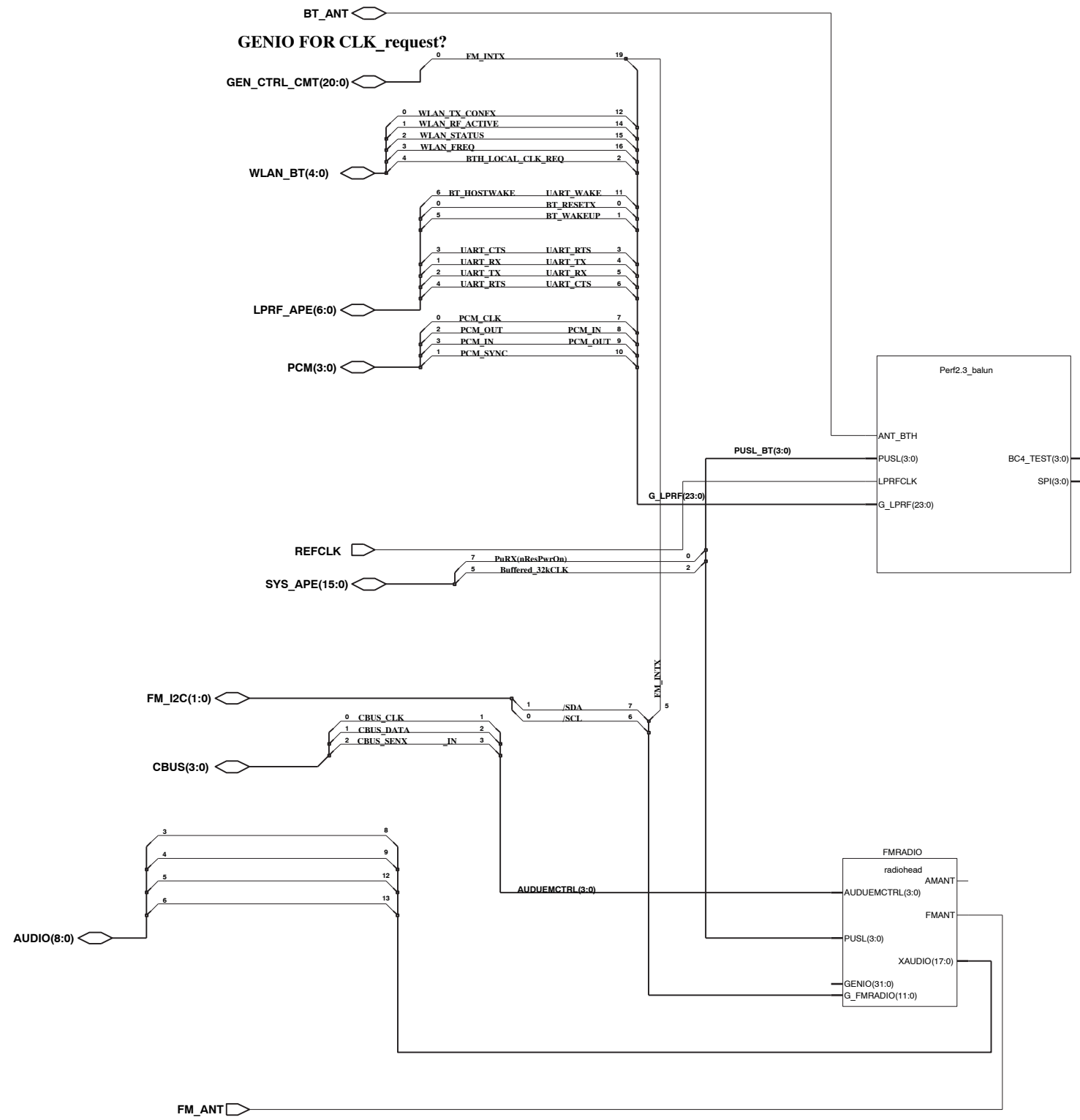
PUSL(7:0) 

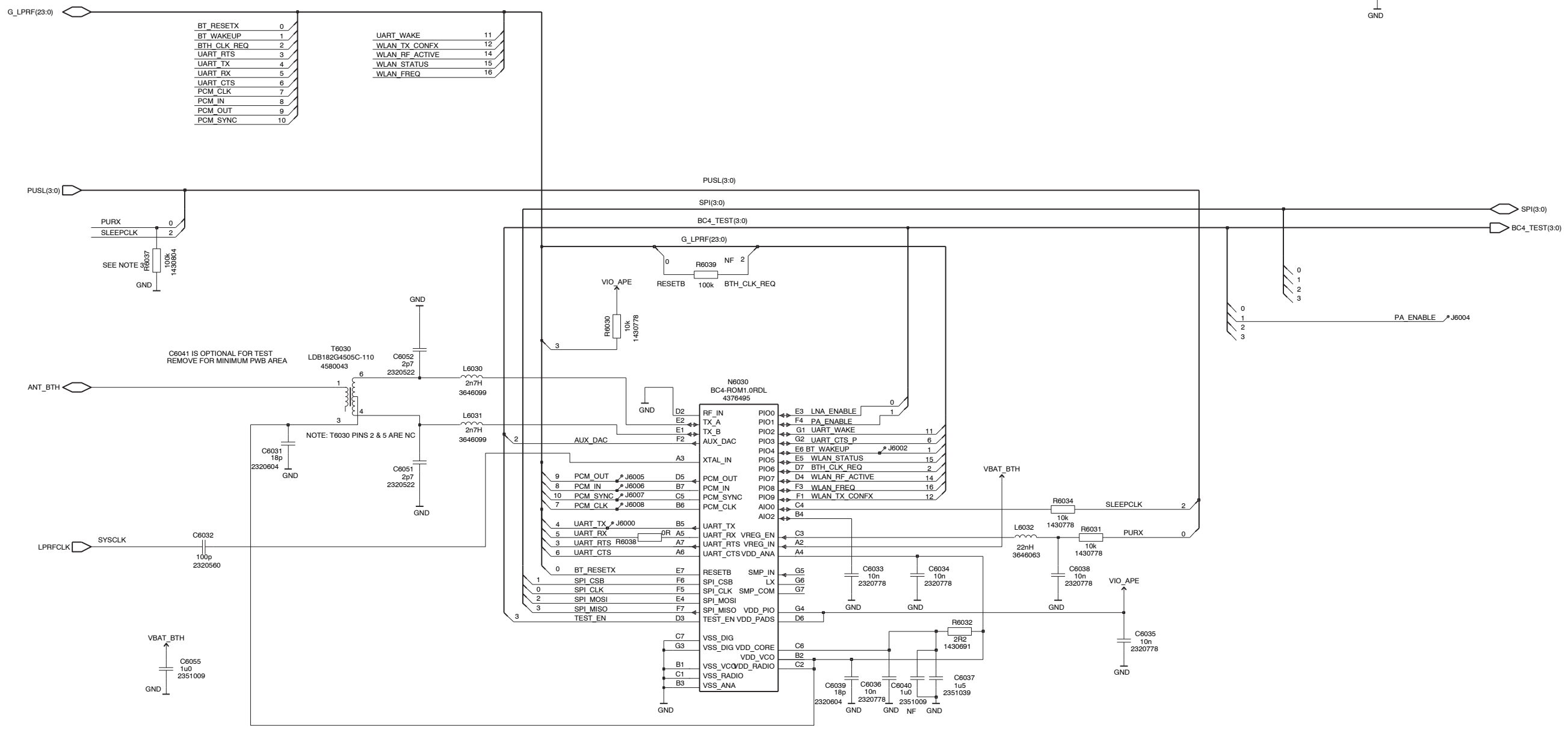
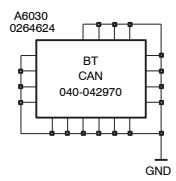


SPI_DVBH(3:0) 









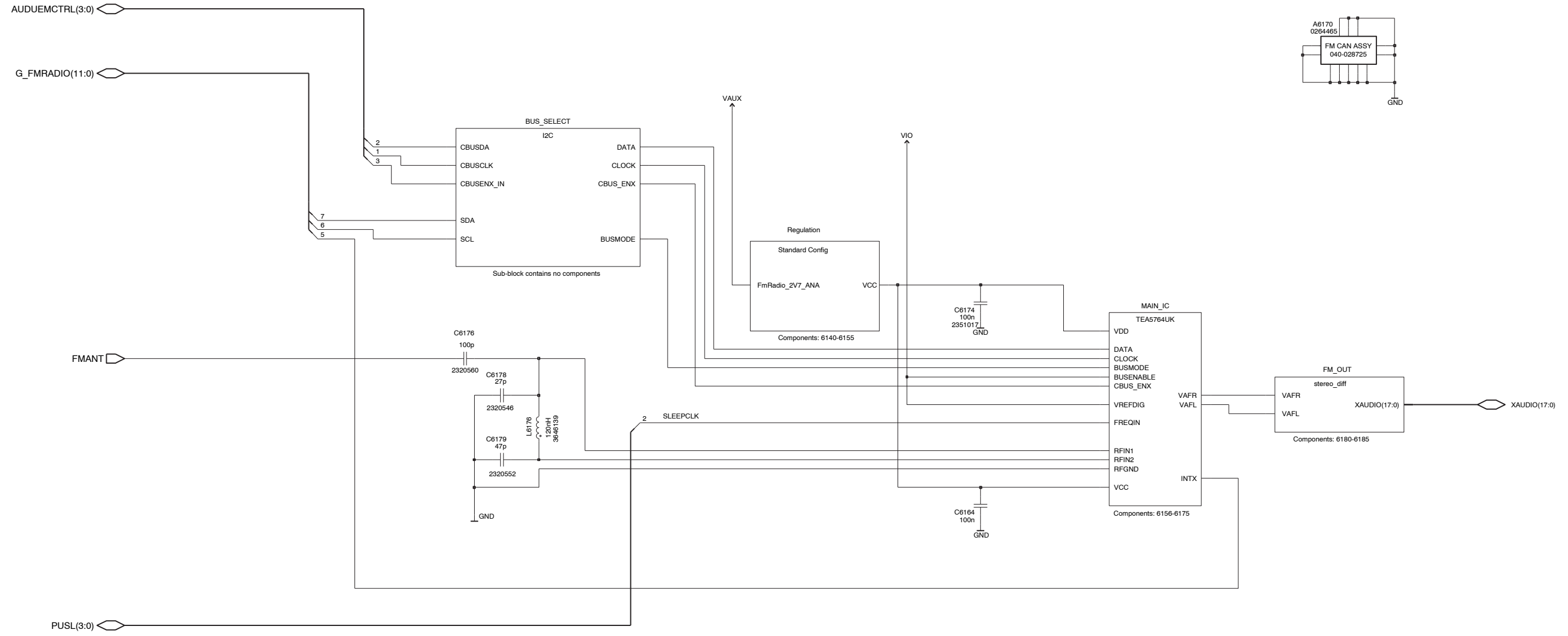
BT RESETX	0
BT WAKEUP	1
BTH_CLK_REQ	2
UART RTS	3
UART TX	4
UART RX	5
UART CTS	6
PCM_CLK	7
PCM_IN	8
PCM_OUT	9
PCM_SYNC	10

UART_WAKE	11
WLAN_TX_CONFX	12
WLAN_RF_ACTIVE	14
WLAN_STATUS	15
WLAN_FREQ	16

C6041 IS OPTIONAL FOR TEST REMOVE FOR MINIMUM PWB AREA

NOTE: T6030 PINS 2 & 5 ARE NC

- Notes
- (1) For EDR testing, provide test pads for UART, PIO1 and RESETX. TEST_EN can be left NC in phone.
 - (2) VREG_EN (C3) is noise sensitive. L6032, R6031, C6038 are required for filtering
 - (3) R6037 may be located where convenient and does not have to be in the Bluetooth area.



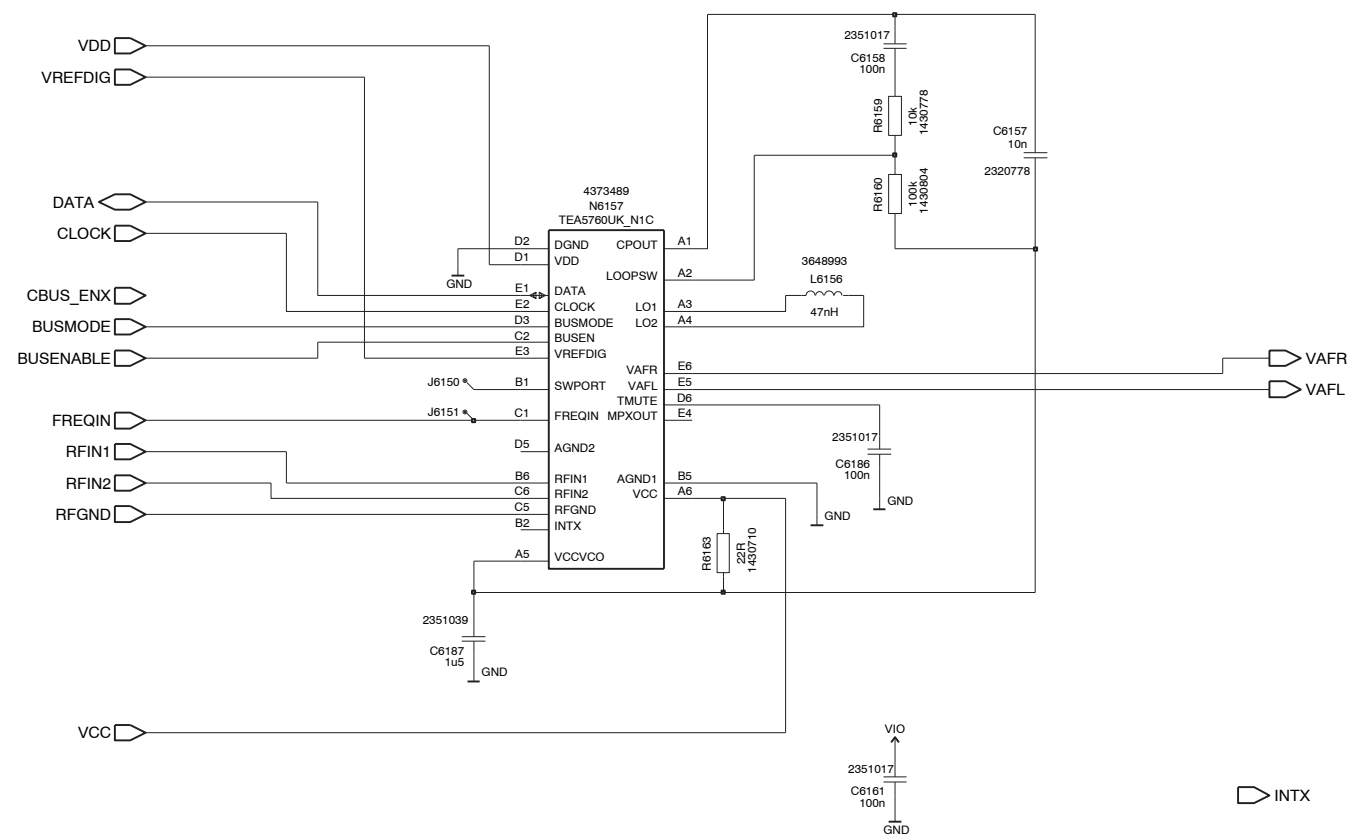
Note: For Layout information, see FM Radio Application Note

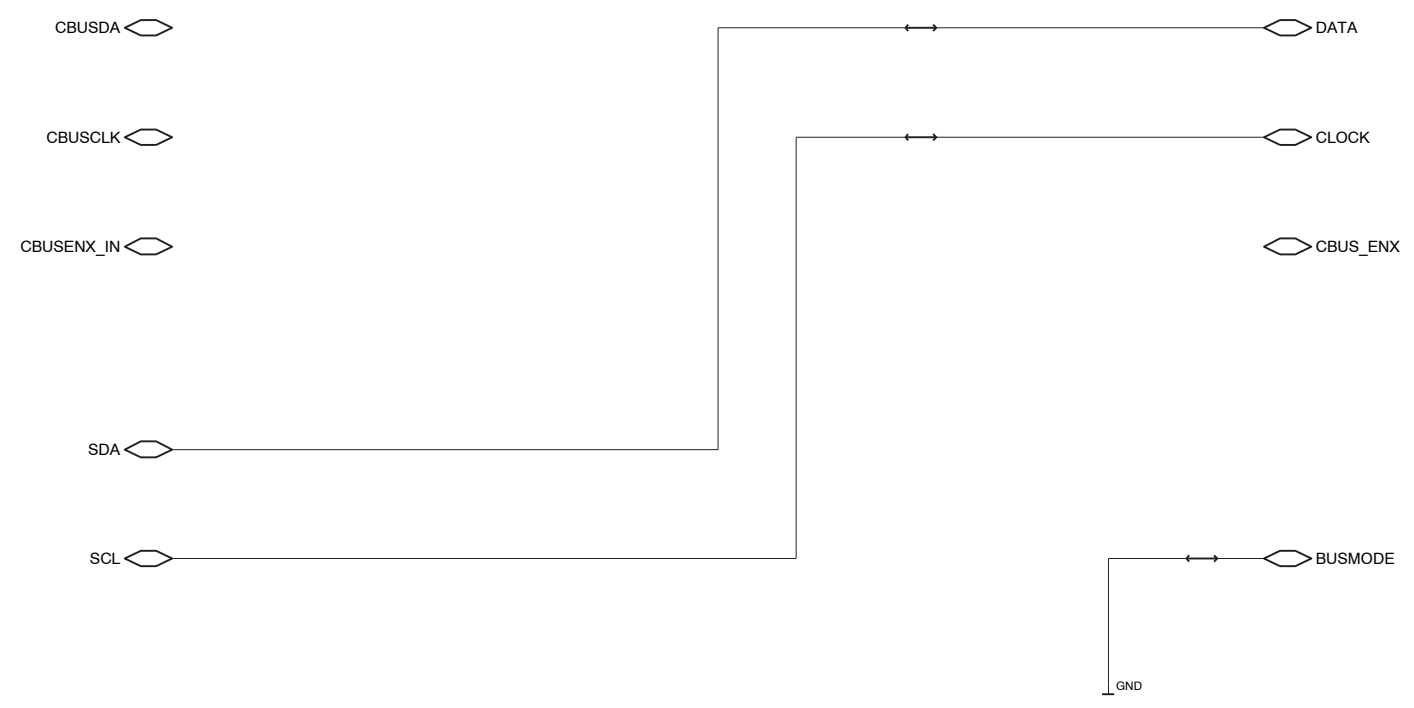
Interface Designation	BB Release	G_MAP sheet Recommended connection(s)	Signal	Function
G_FMRADIO(5)	BB4.0	GENIO(24)	INTX	Falling Edge Interrupt
	BB4.5	GENIO(8) or GENIO(9) or GENIO(10) or GENIO(11)		
FmRadio_2V7_ANA		VANA	VCC/VDD	Main 2.7Vdc Supply
FmRadio_1V8_Dig		VIO	VREFDIG	1.8Vdc IO Supply

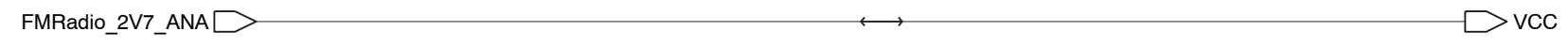
Radiohead Component Allocation: 6100-6199

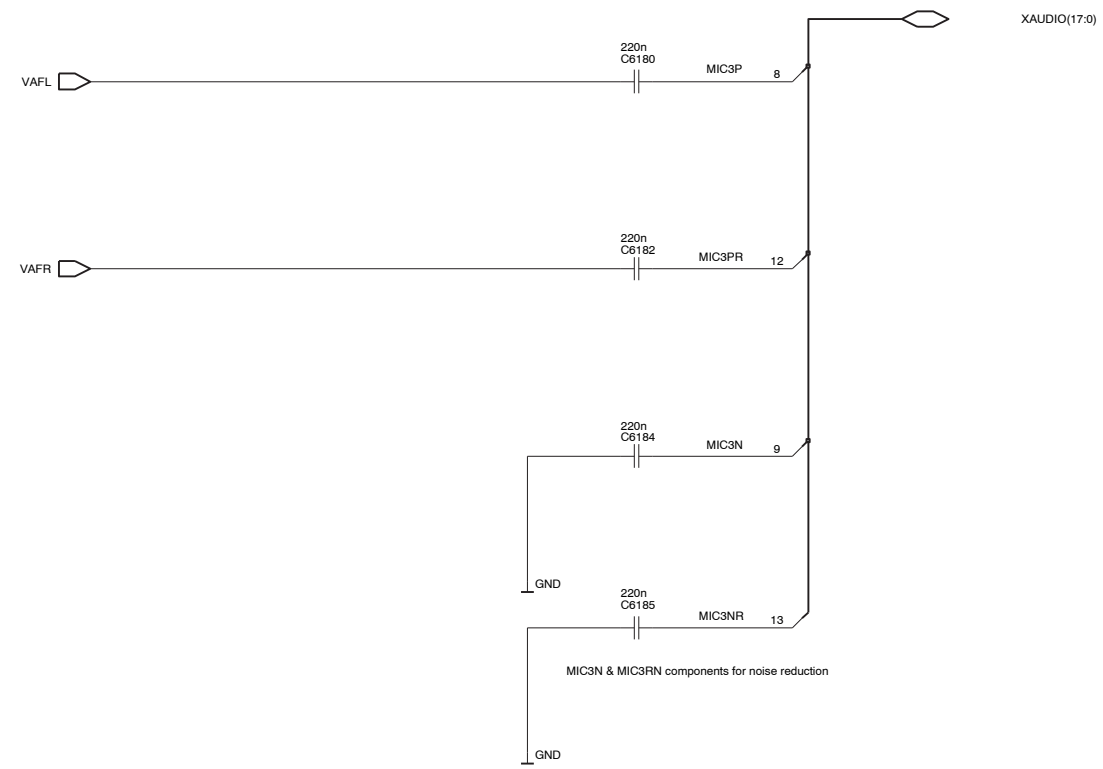
AMANT

GENIO(31:0)

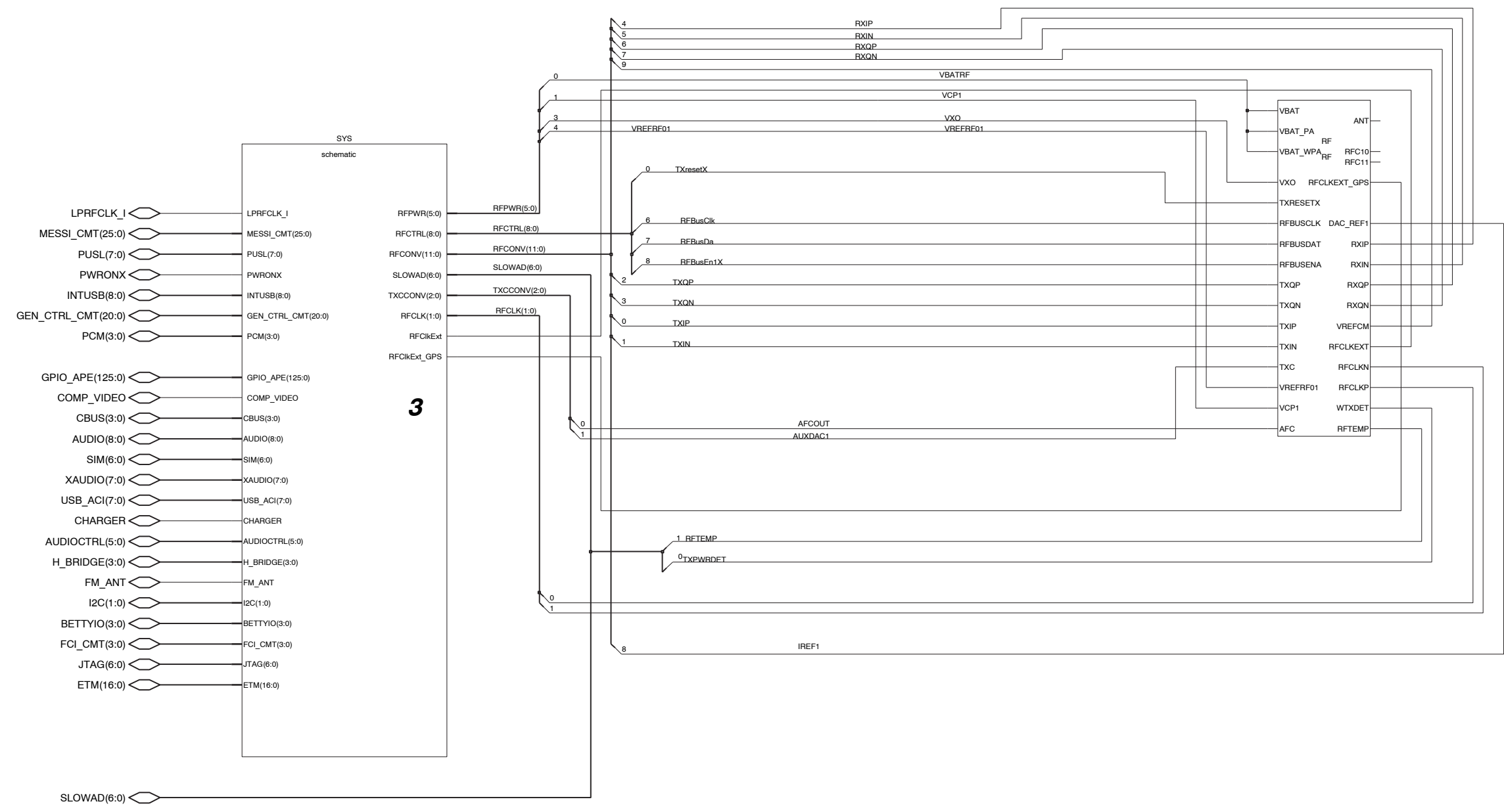


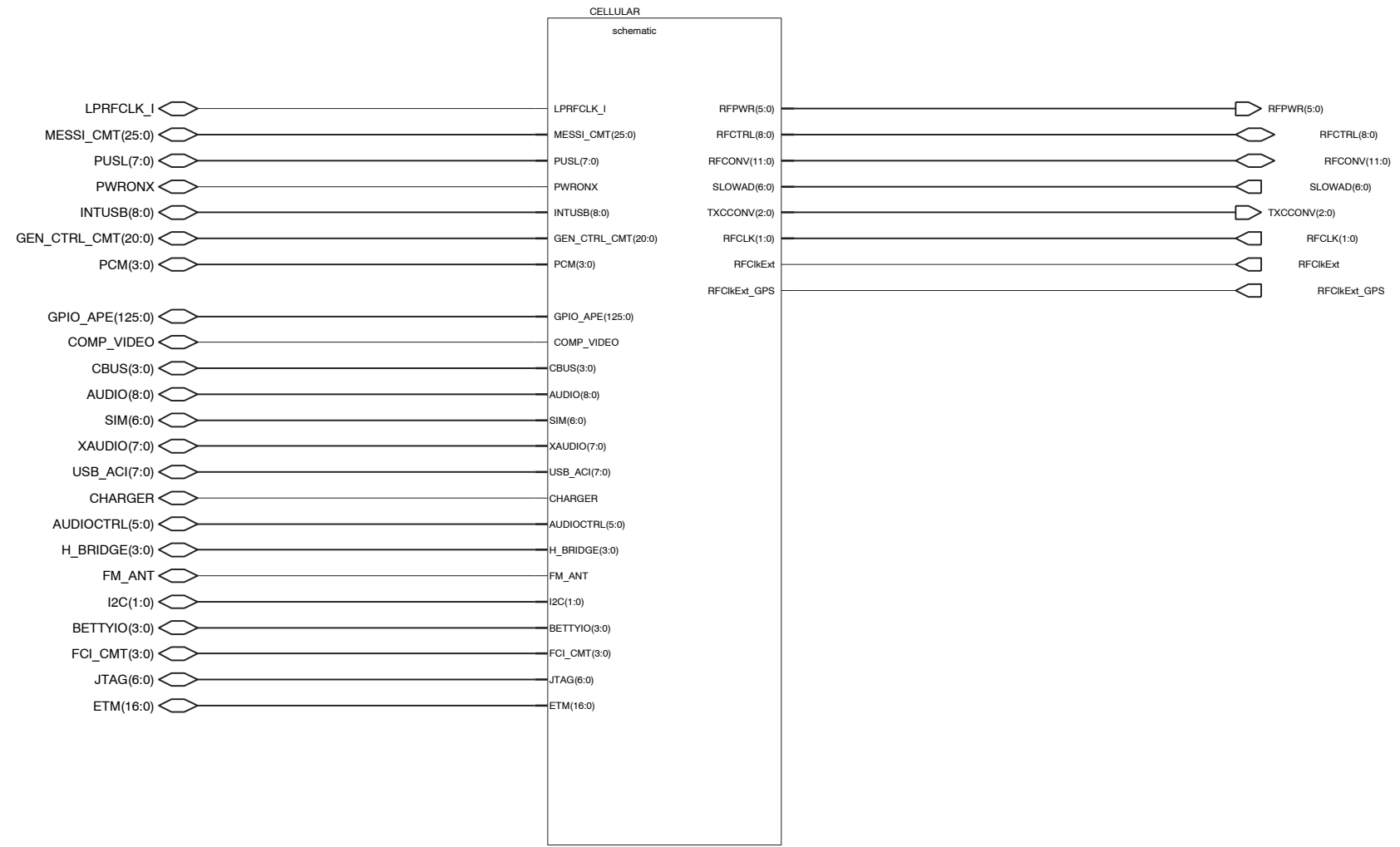


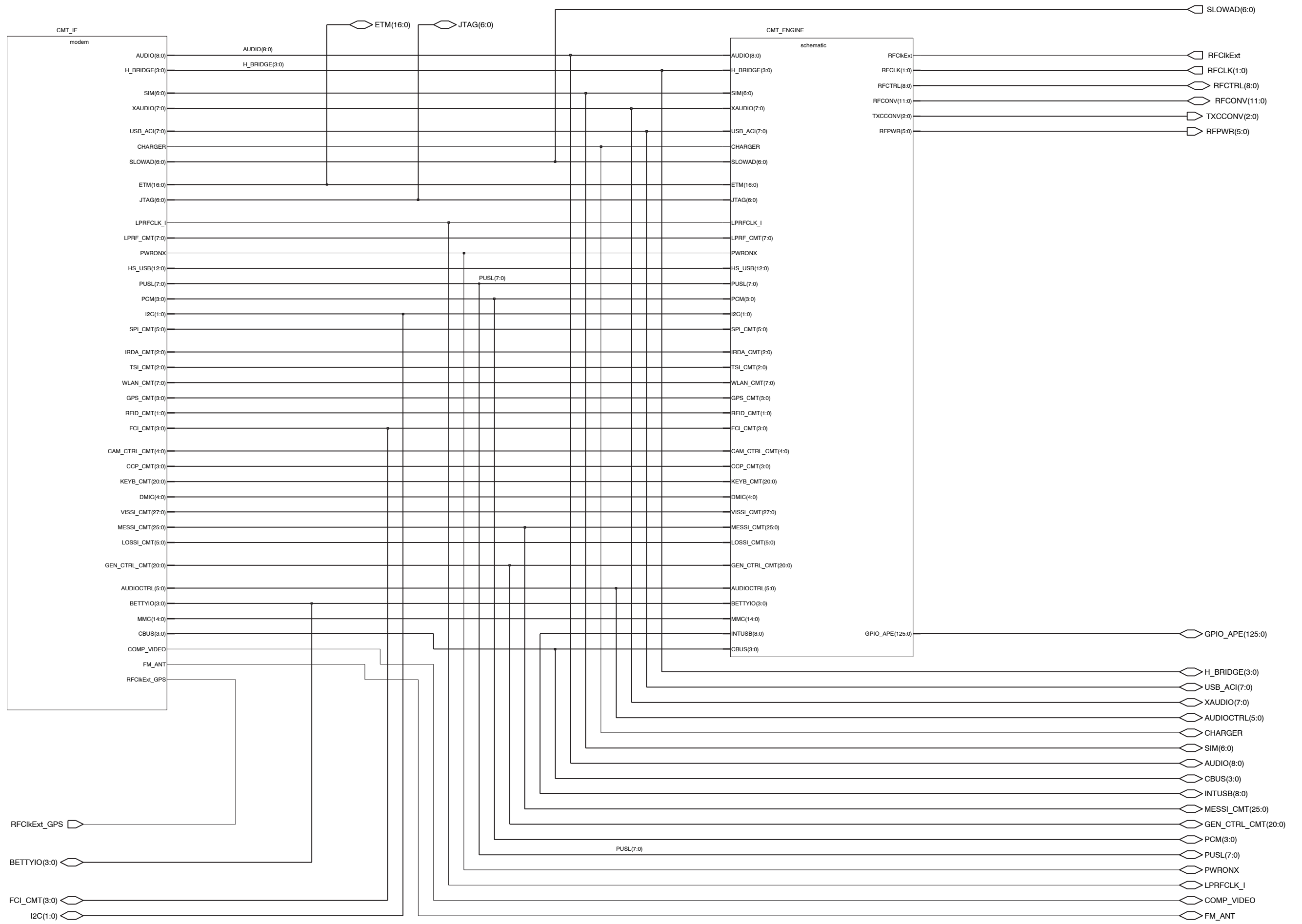


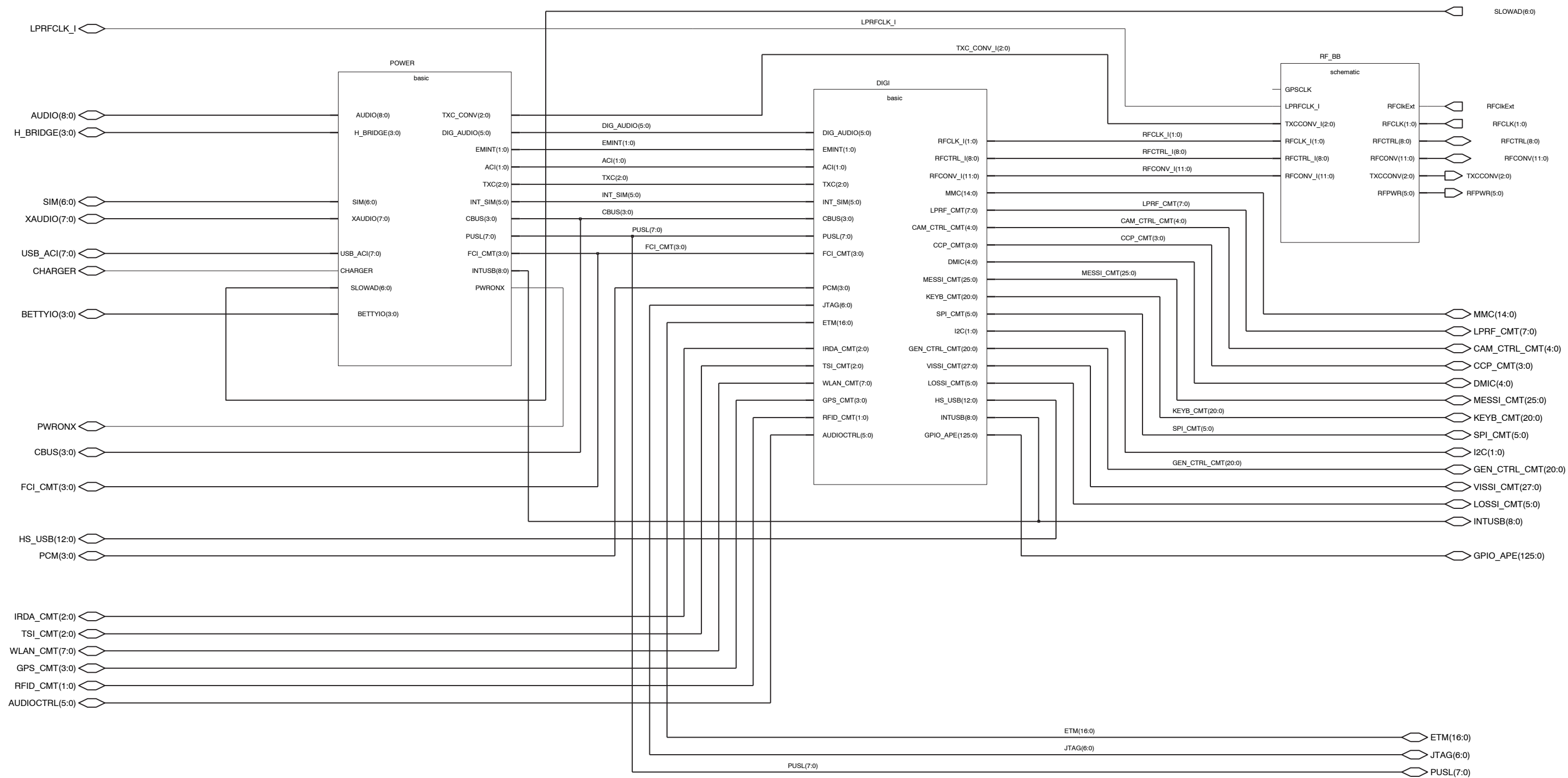


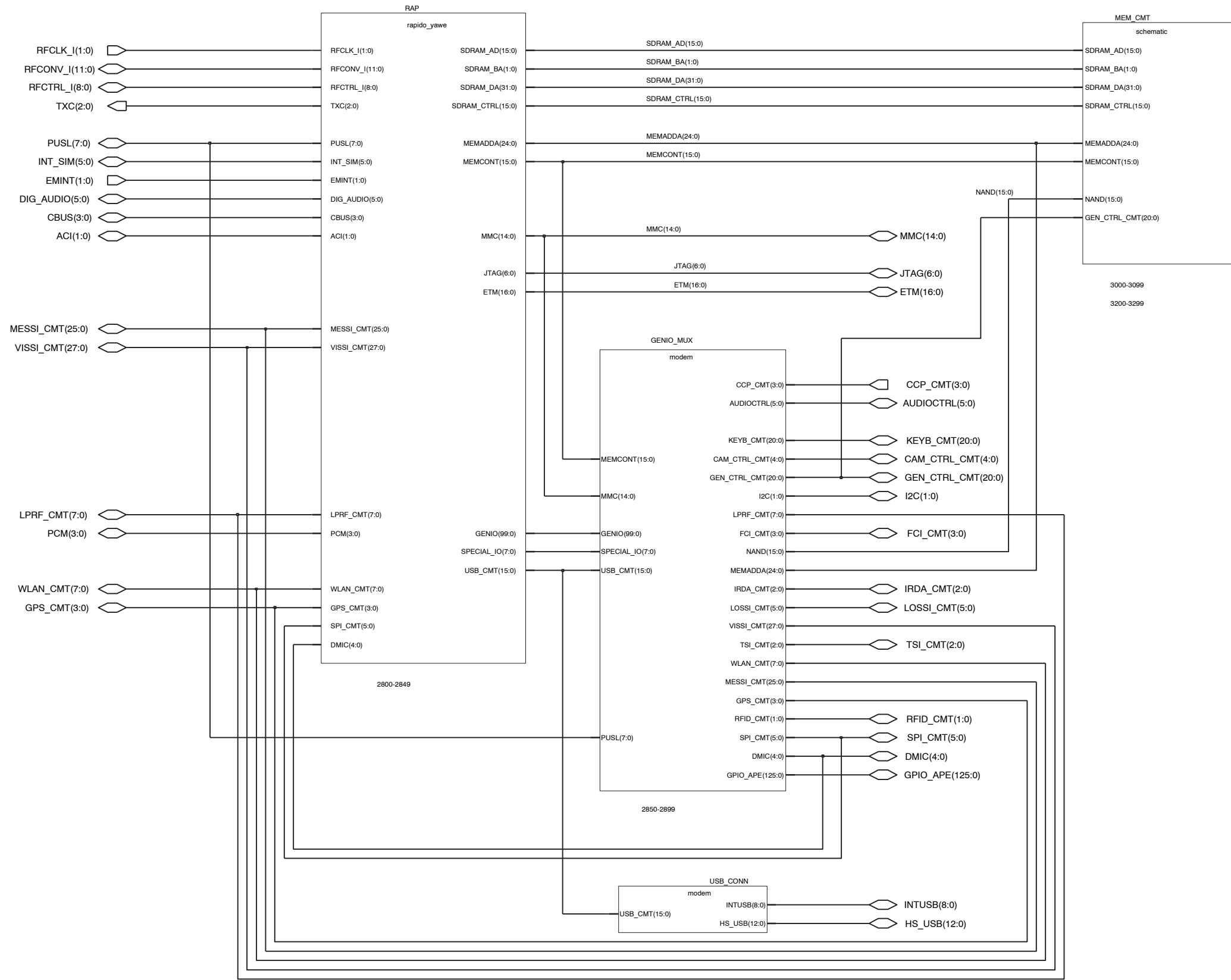
For use with UEME and audio circuits with true differential inputs

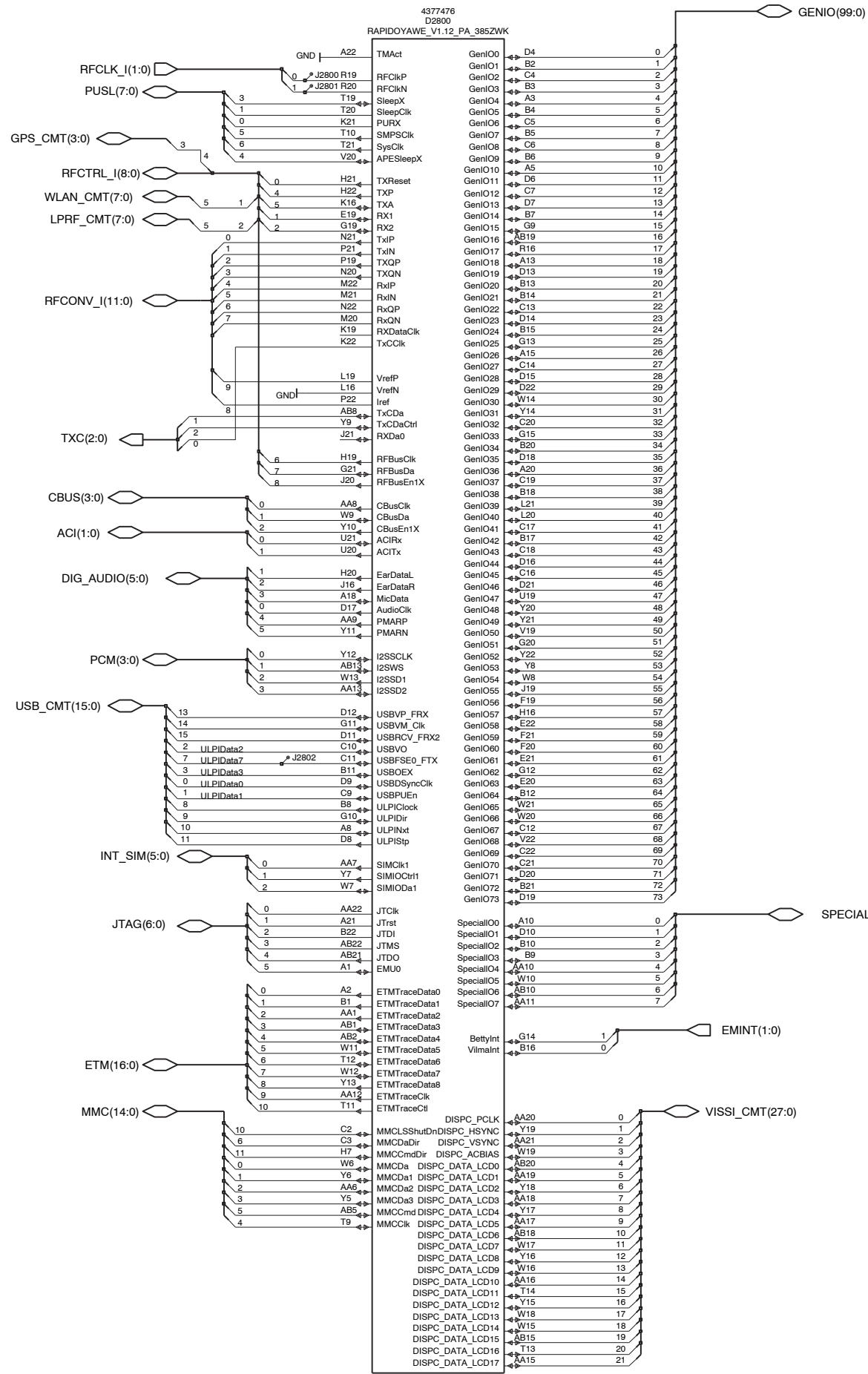




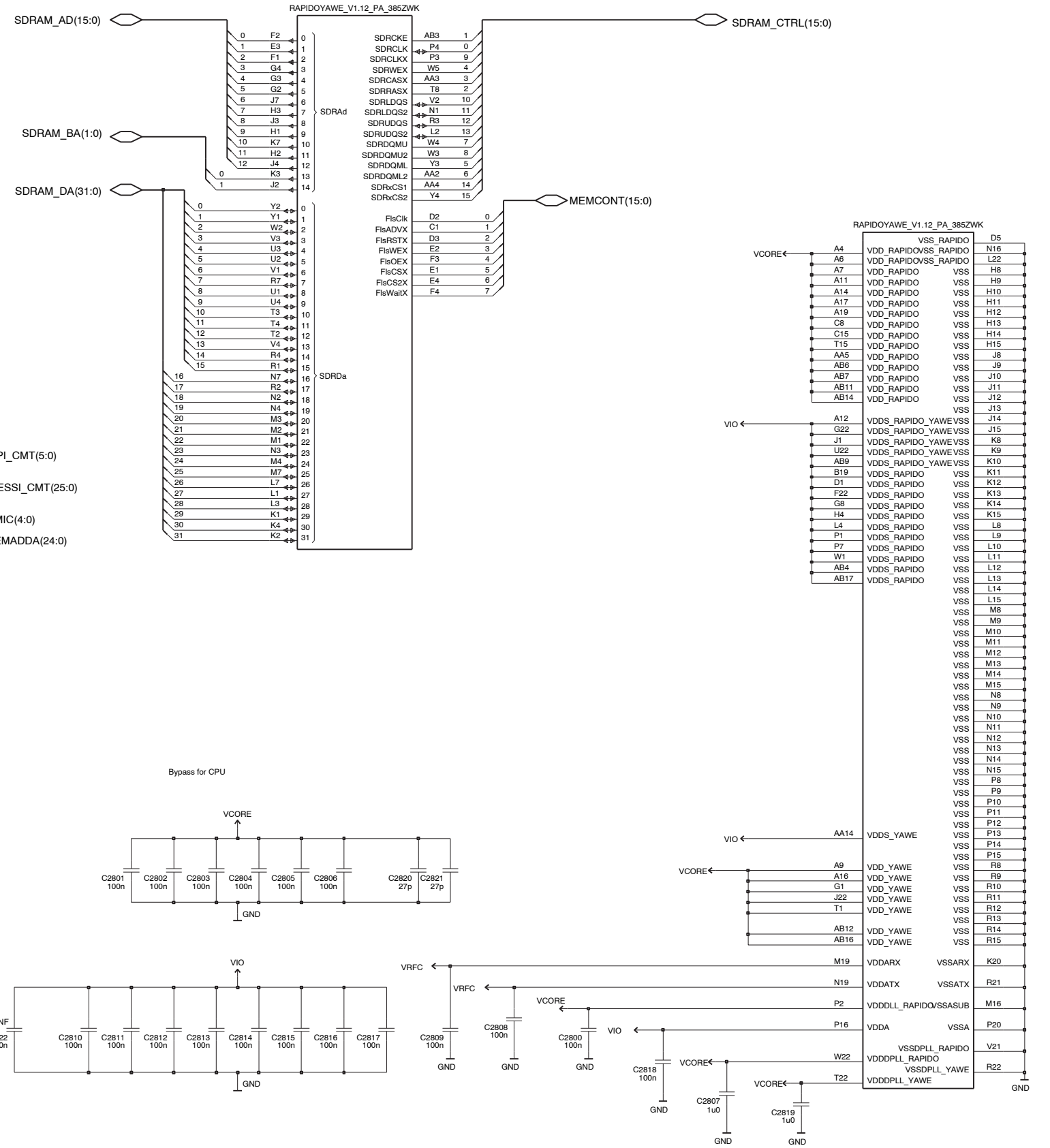


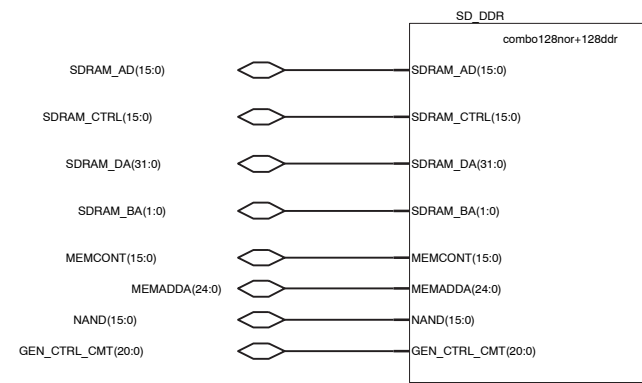




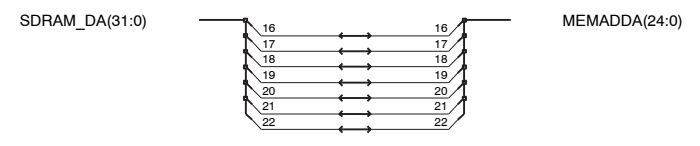
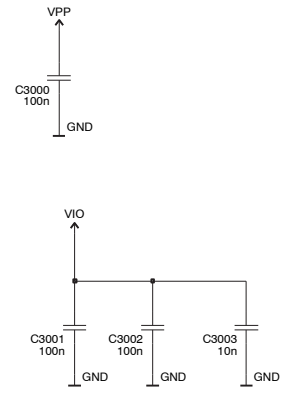


- SPI_CMT(5:0)
- MESSI_CMT(25:0)
- DMIC(4:0)
- MEMADDA(24:0)

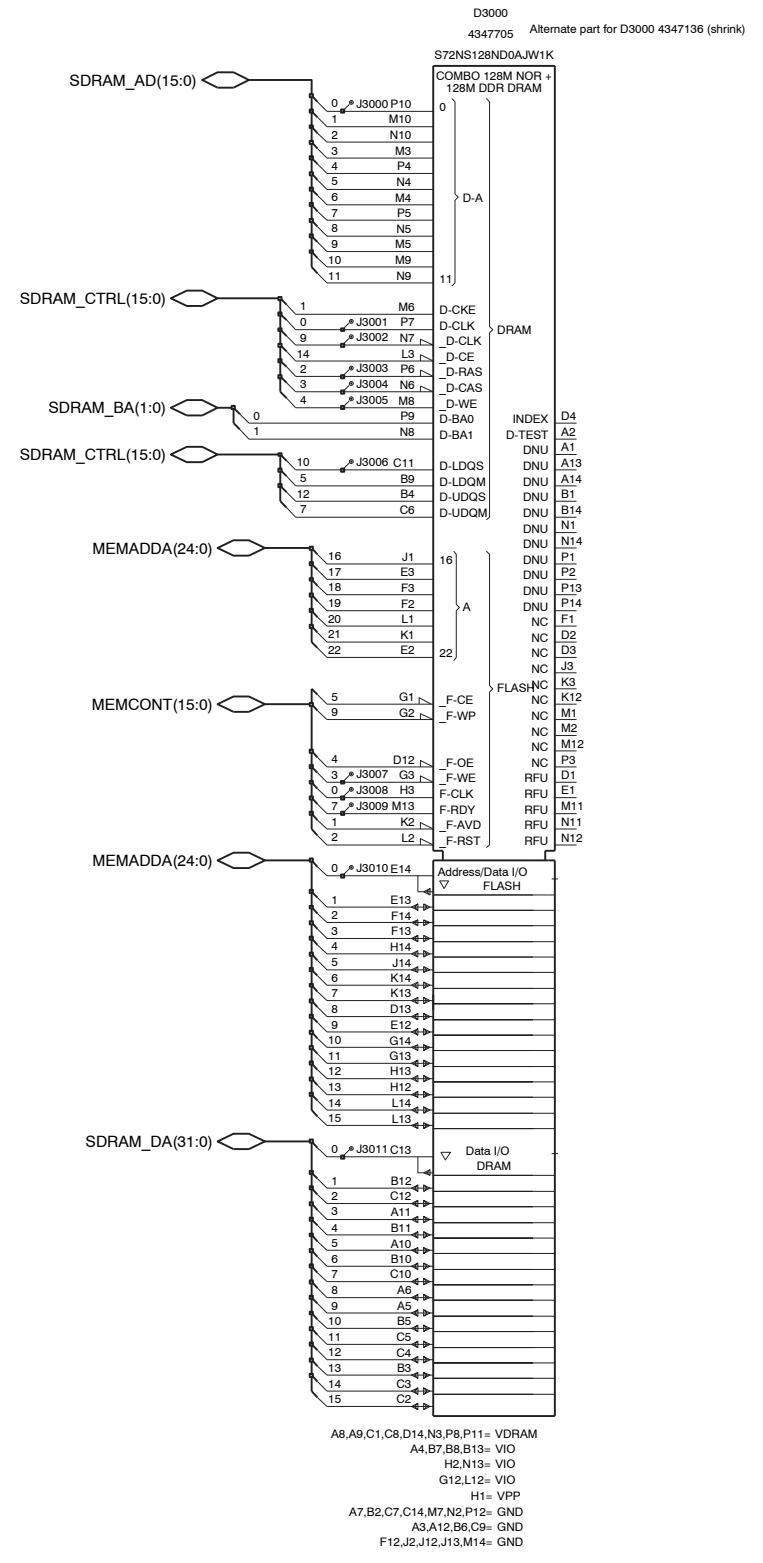
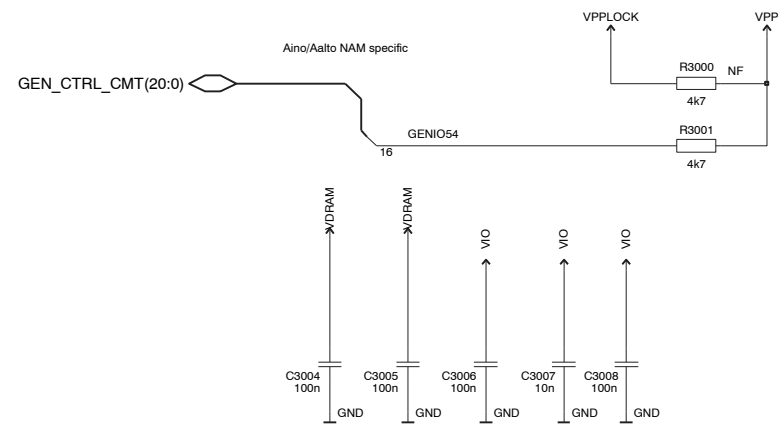


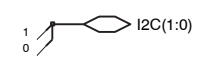
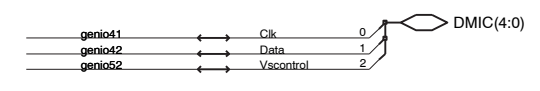
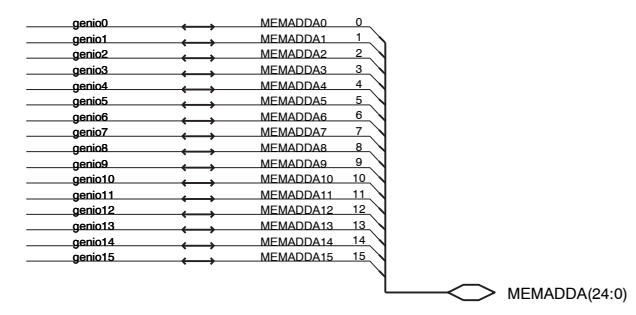
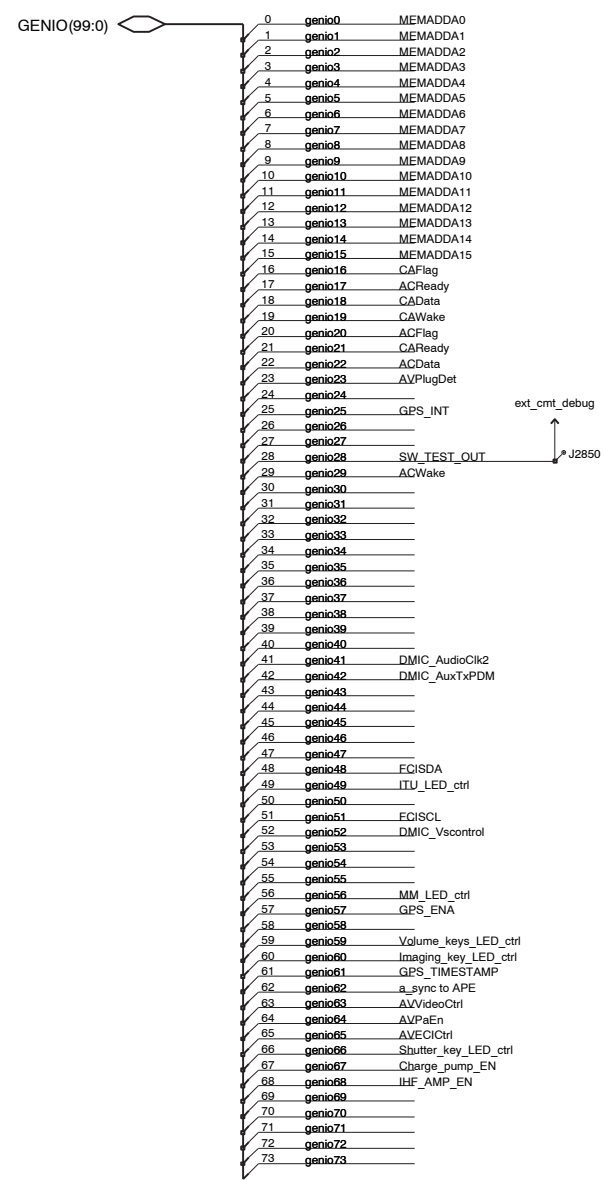


NAND(15:0)

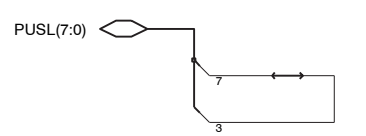
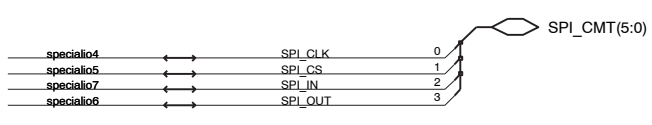
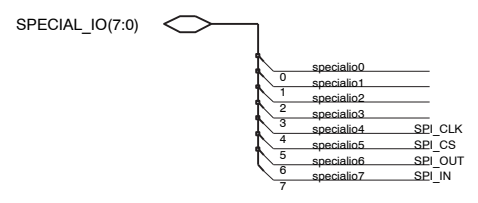
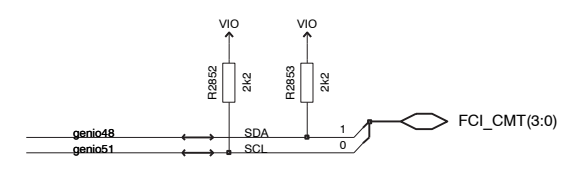
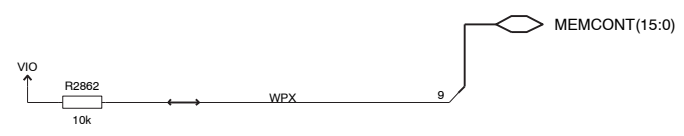
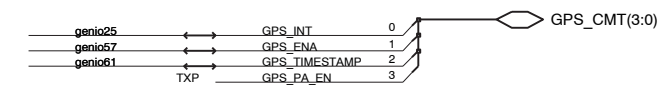


NOTE: MEMADDA(24:16) IS MUXED TO SDRAM_DA(24:16) IN RAPIDOYAWE



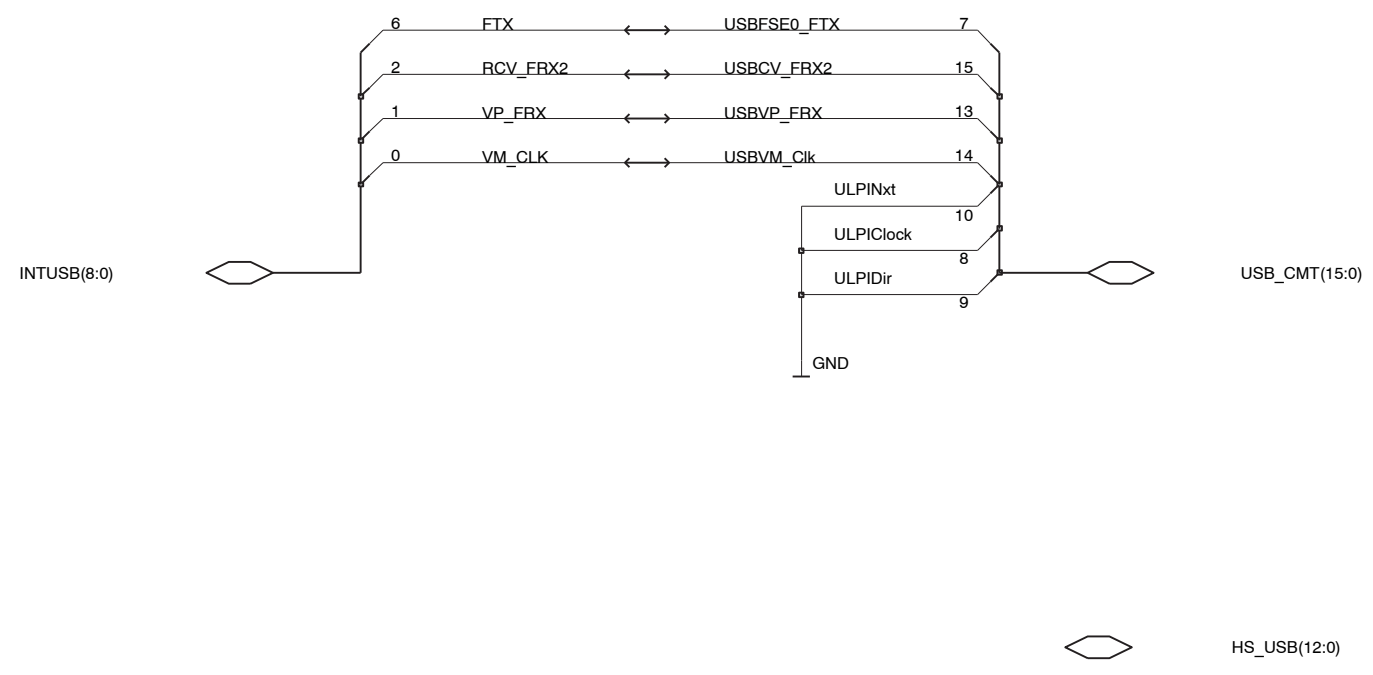


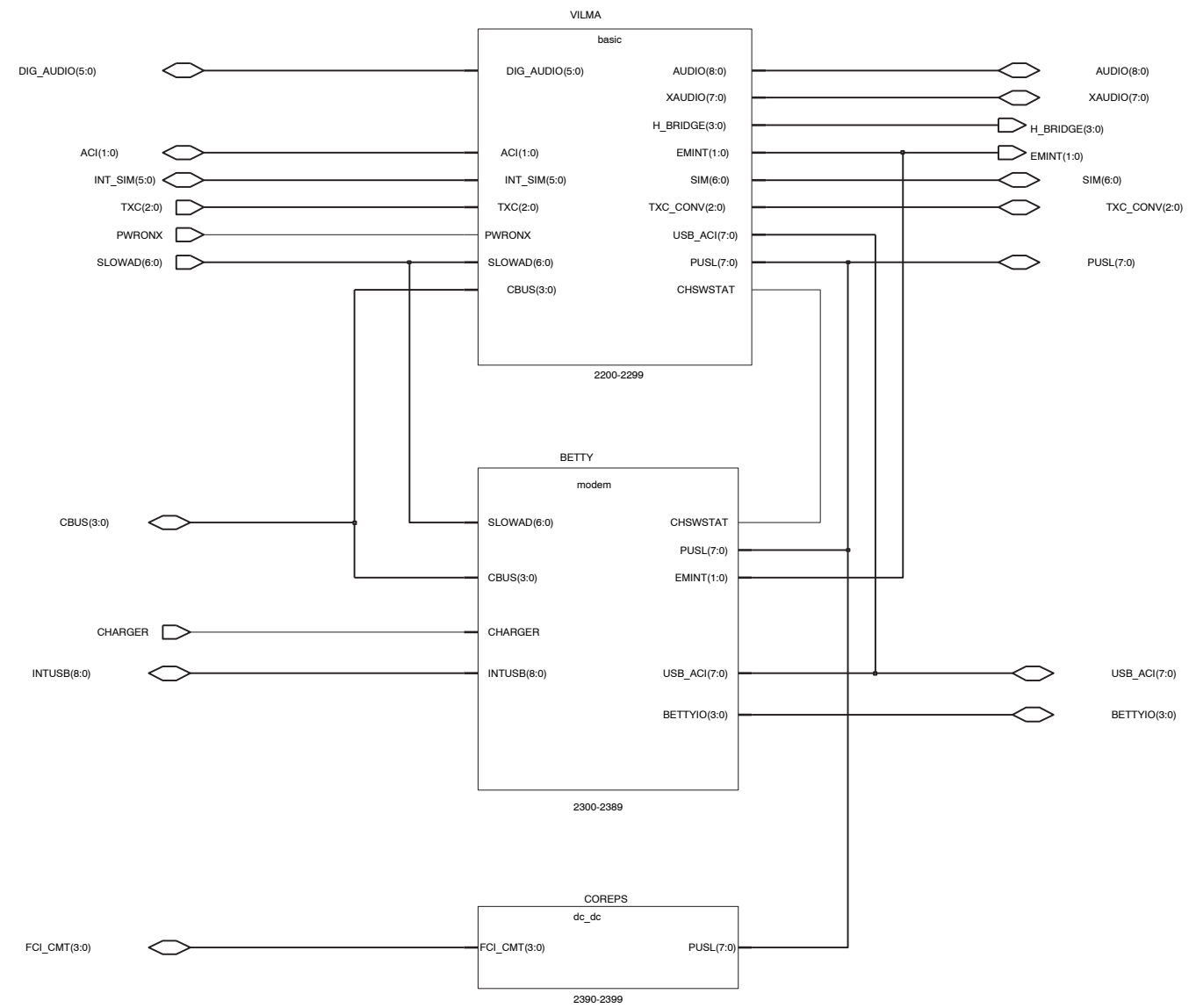
Note: GPS controls are to be changed

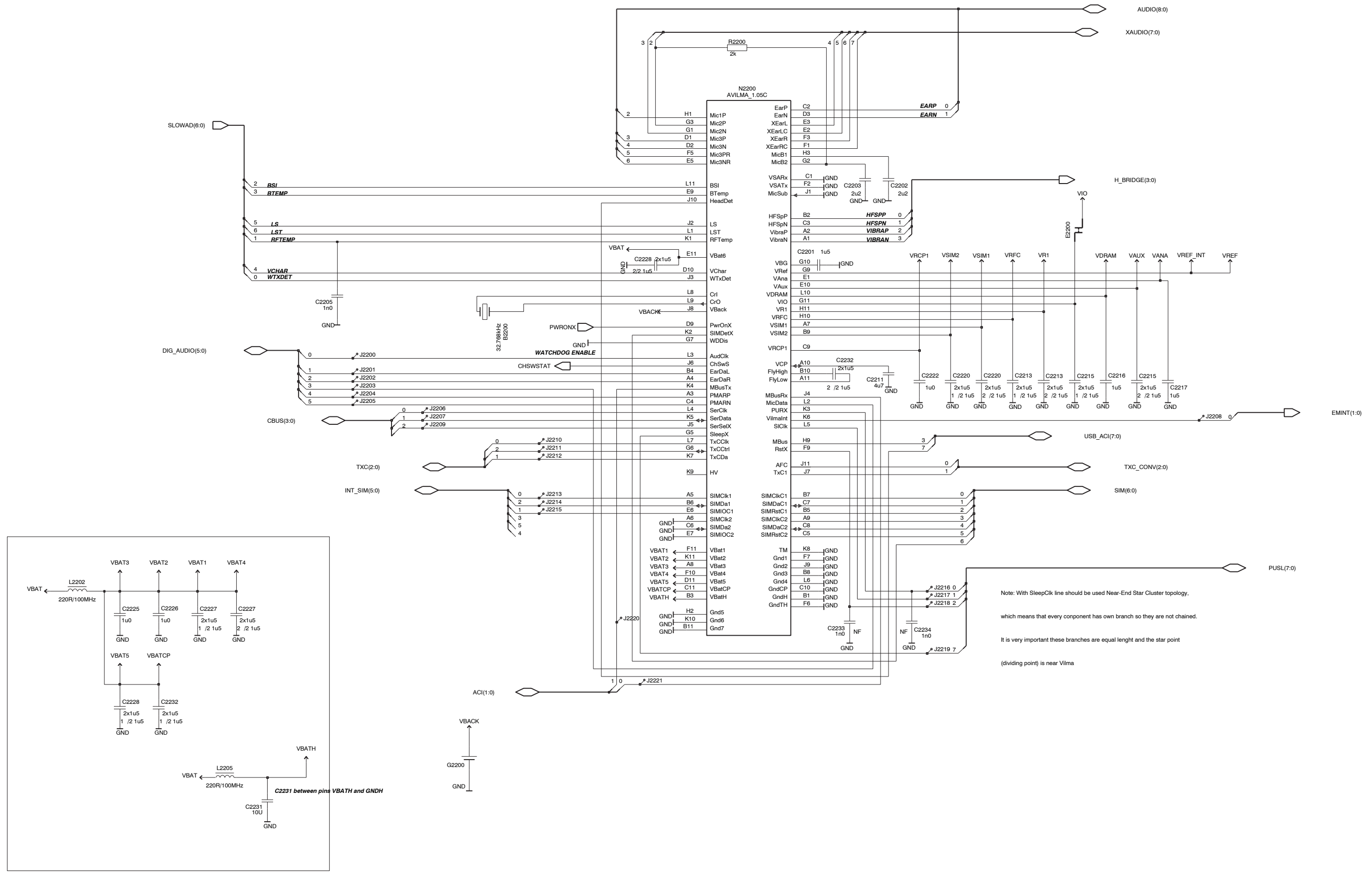


IF EXTERNAL CLOCK REQUESTS ARE NOT USED
PUSL LINES 7 AND 3 MUST BE CONNECTED

- FCI_CMT(3:0)
- SPI_CMT(5:0)
- RFID_CMT(1:0)
- USB_CMT(15:0)
- LPRF_CMT(7:0)
- TSI_CMT(2:0)
- KEYB_CMT(20:0)
- NAND(15:0)
- CAM_CTRL_CMT(4:0)
- MMC(14:0)
- LOSSI_CMT(5:0)
- WLAN_CMT(7:0)
- SPI_CMT(5:0)
- IRDA_CMT(2:0)
- VISSI_CMT(27:0)
- CCP_CMT(3:0)



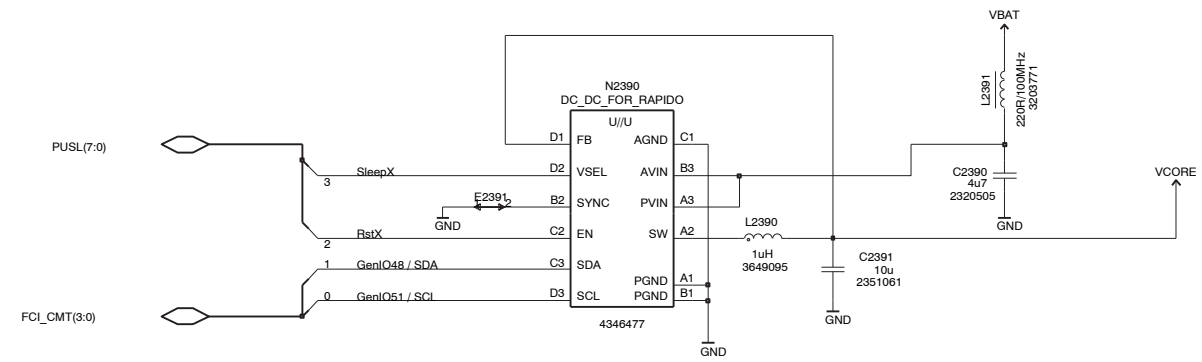


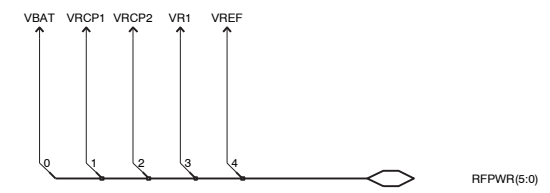
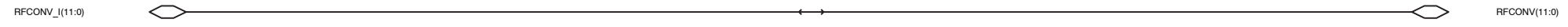
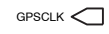
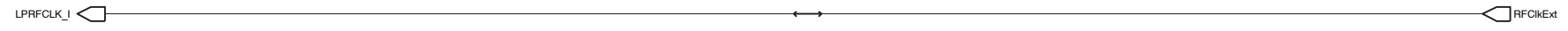
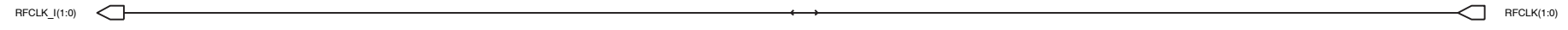


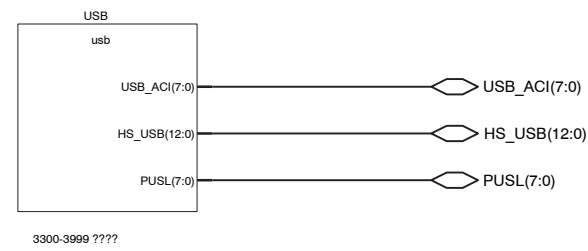
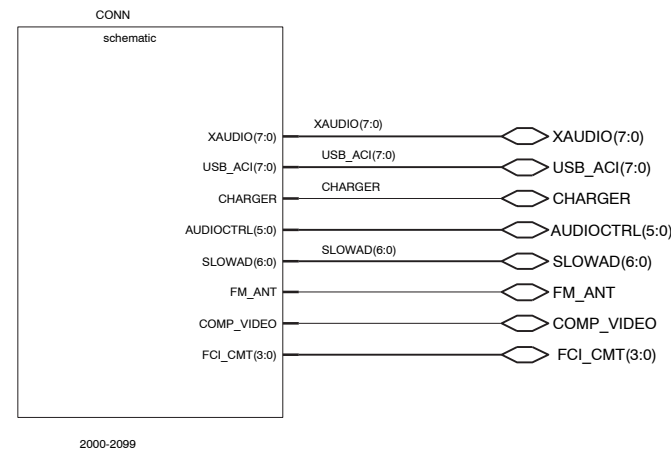
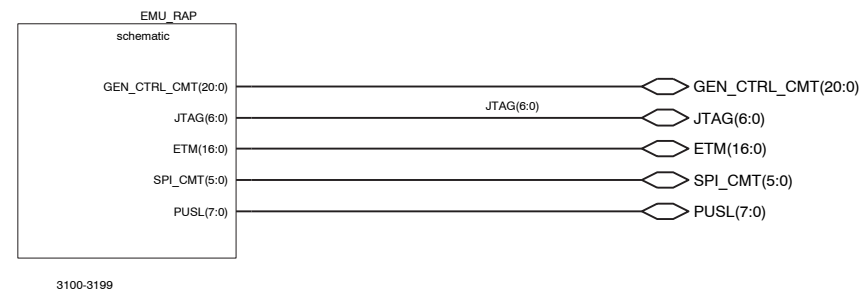
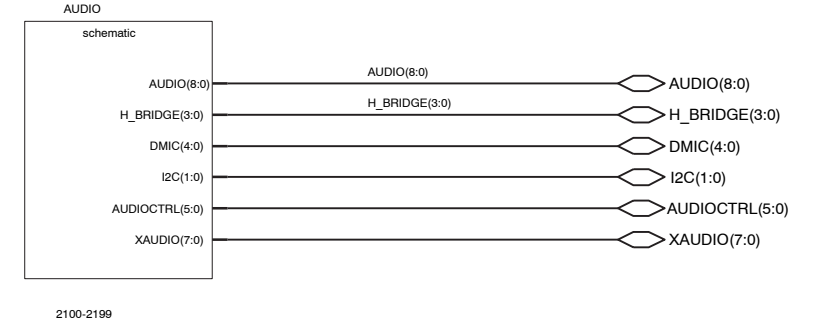
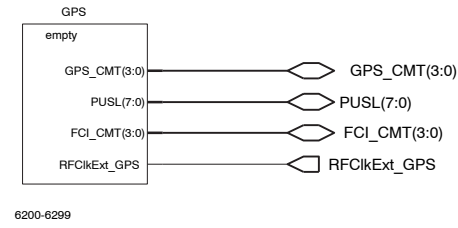
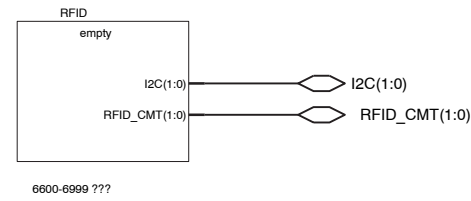
Note: With SleepCik line should be used Near-End Star Cluster topology, which means that every component has own branch so they are not chained. It is very important these branches are equal length and the star point (dividing point) is near Vilma

Reference schematic

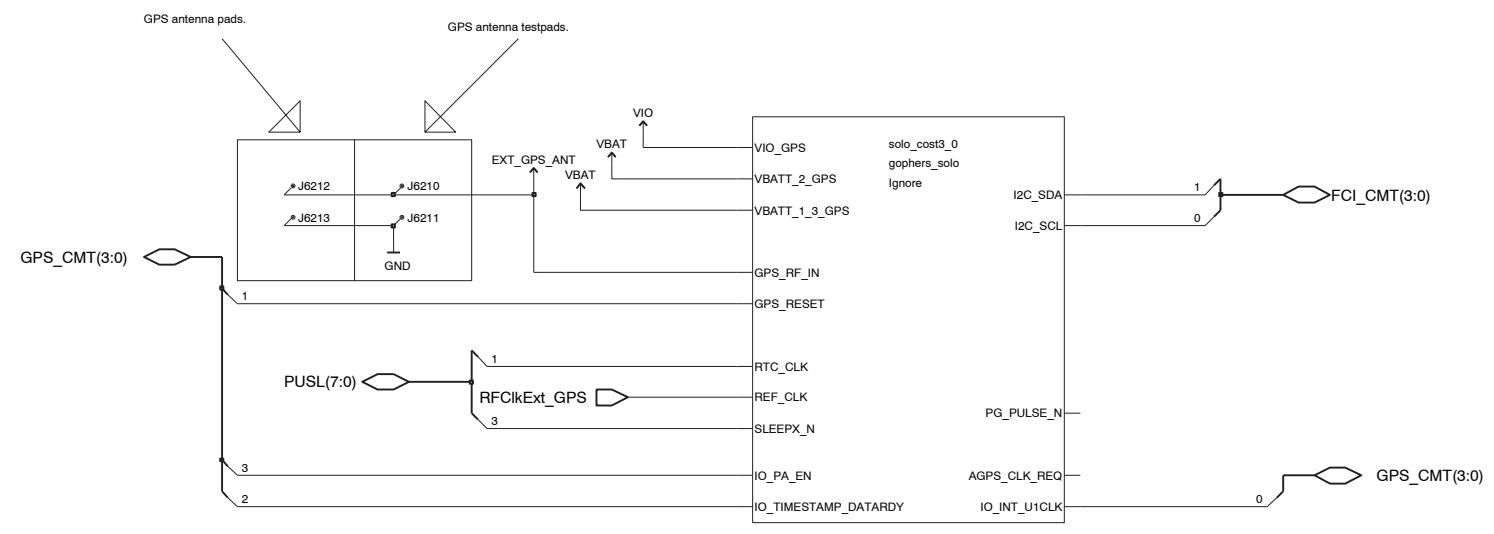
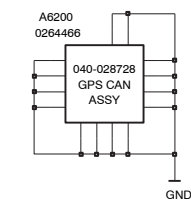
NOTE! SDA and SCL lines should include 10-47kOhm pull up resistors. Resistors value is dependent on number of I2C slaves

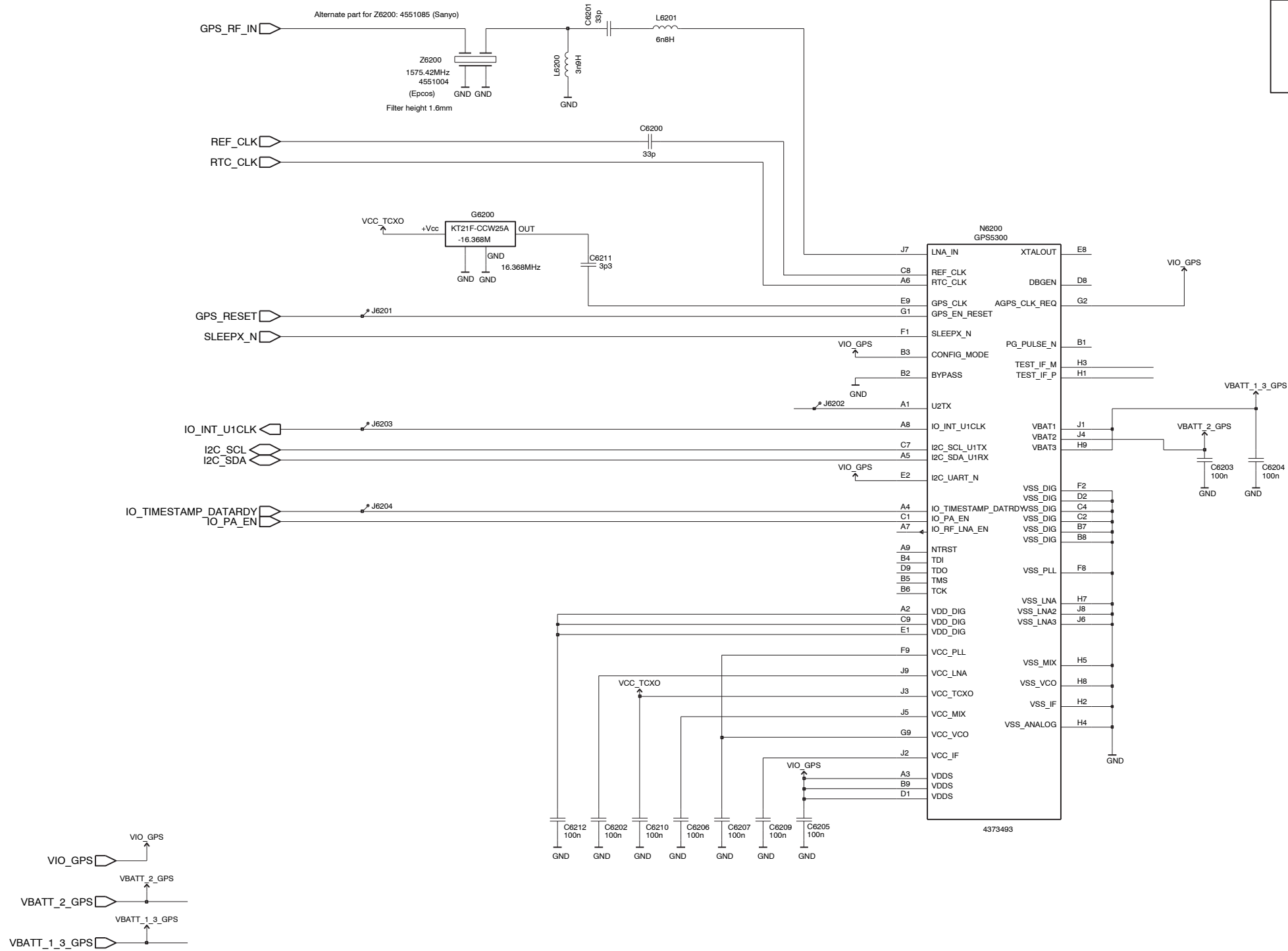






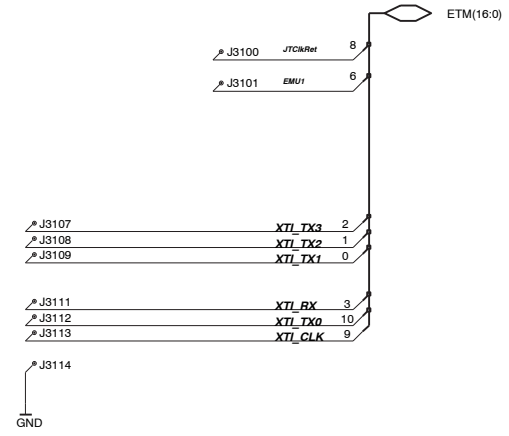
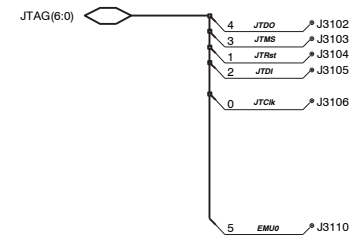
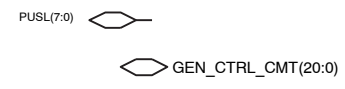
- ◊ PWRONX
- ◊ SLOWAD(6:0)
- ◊ VISSI_CMT(27:0)
- ◊ MESSI_CMT(25:0)
- ◊ LOSSI_CMT(5:0)
- ◊ KEYB_CMT(20:0)
- ◊ SPI_CMT(5:0)
- ◊ FCI_CMT(3:0)
- ◊ TSI_CMT(2:0)
- ◊ BETTYIO(3:0)
- ◊ SIM(6:0)
- ◊ MMC(14:0)
- ◊ I2C(1:0)
- ◊ PUSL(7:0)
- ◊ GEN_CTRL_CMT(20:0)
- ◊ COMP_VIDEO
- ◊ CCP_CMT(3:0)
- ◊ CAM_CTRL_CMT(4:0)
- ◊ USB_ACI(7:0)
- ◊ HS_USB(12:0)
- ◊ IRDA_CMT(2:0)
- ◊ FM_ANT
- ◊ AUDIO(8:0)
- ◊ PCM(3:0)
- ◊ LPRF_CMT(7:0)
- ◊ LPRFCLK_I
- ◊ WLAN_CMT(7:0)
- ◊ PCM(3:0)
- ◊ CBUS(3:0)

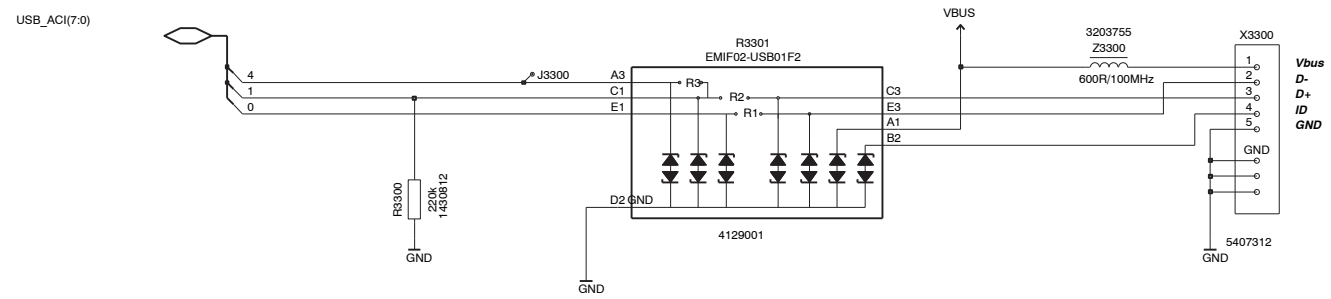




PIN	CONNECT TO	
	VIO_GPS	GND
I2C_UART_N	I2C MODE	UART MODE
BYPASS	CLOCK SLICER BYPASSED MODE [REF_CLK IS DIGITAL]	CLOCK SLICER ENABLED MODE [REF_CLK IS ANALOG]

AGPS_CLK_REQ
 PG_PULSE_N







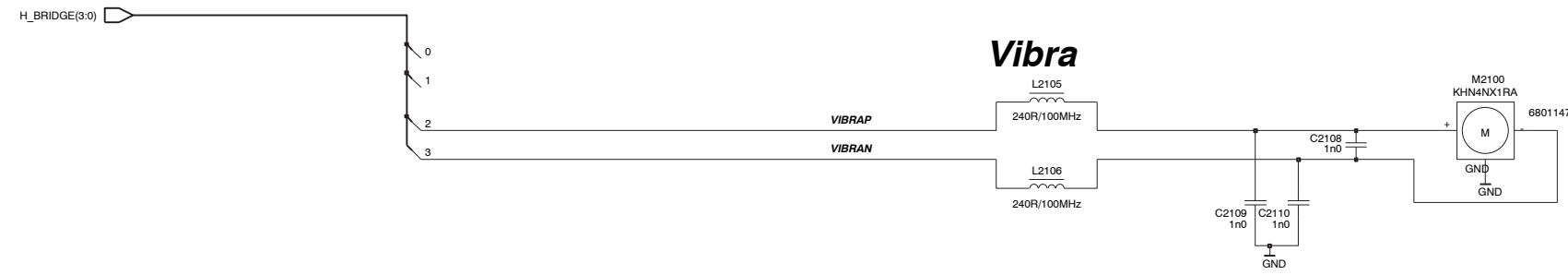
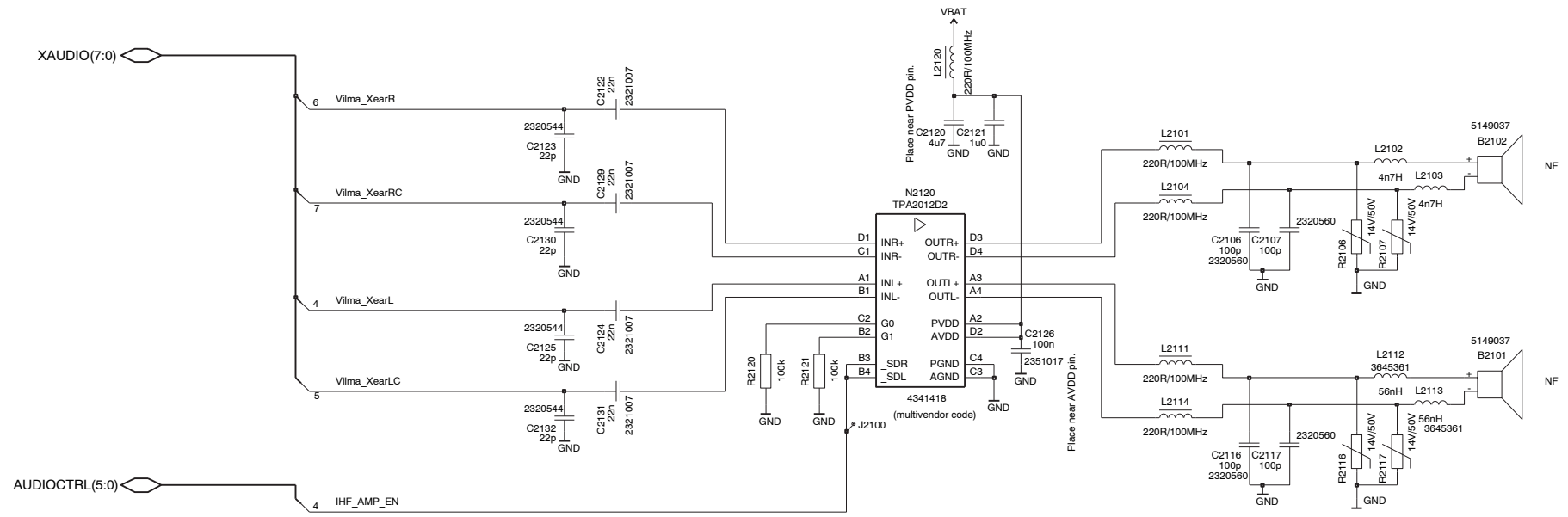
USB_ACI(7:0)

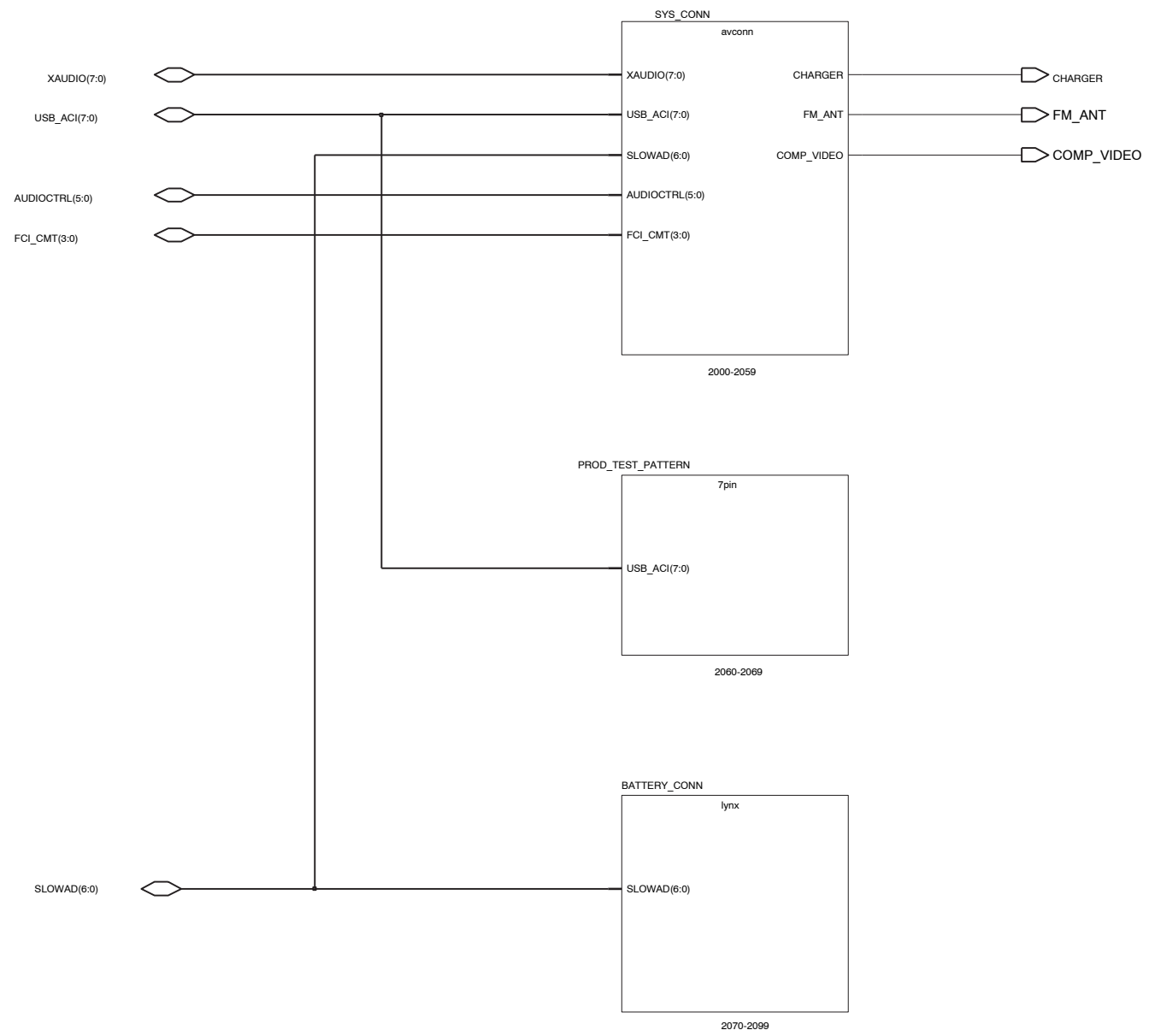
HS_USB(12:0)

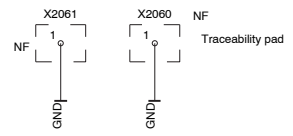
PUSL(7:0)

DMIC(4:0) 
I2C(1:0) 

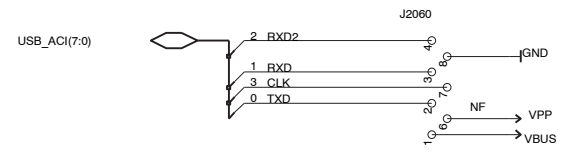
IHF- connection

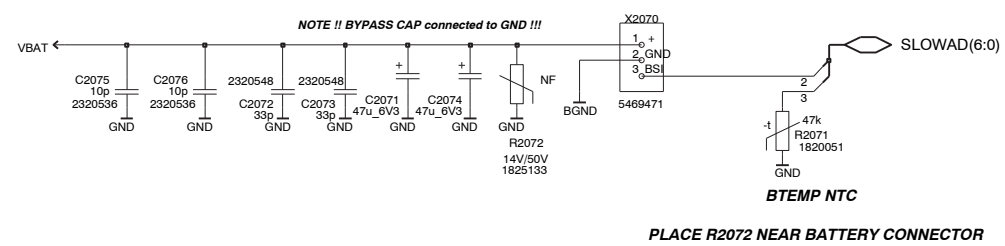


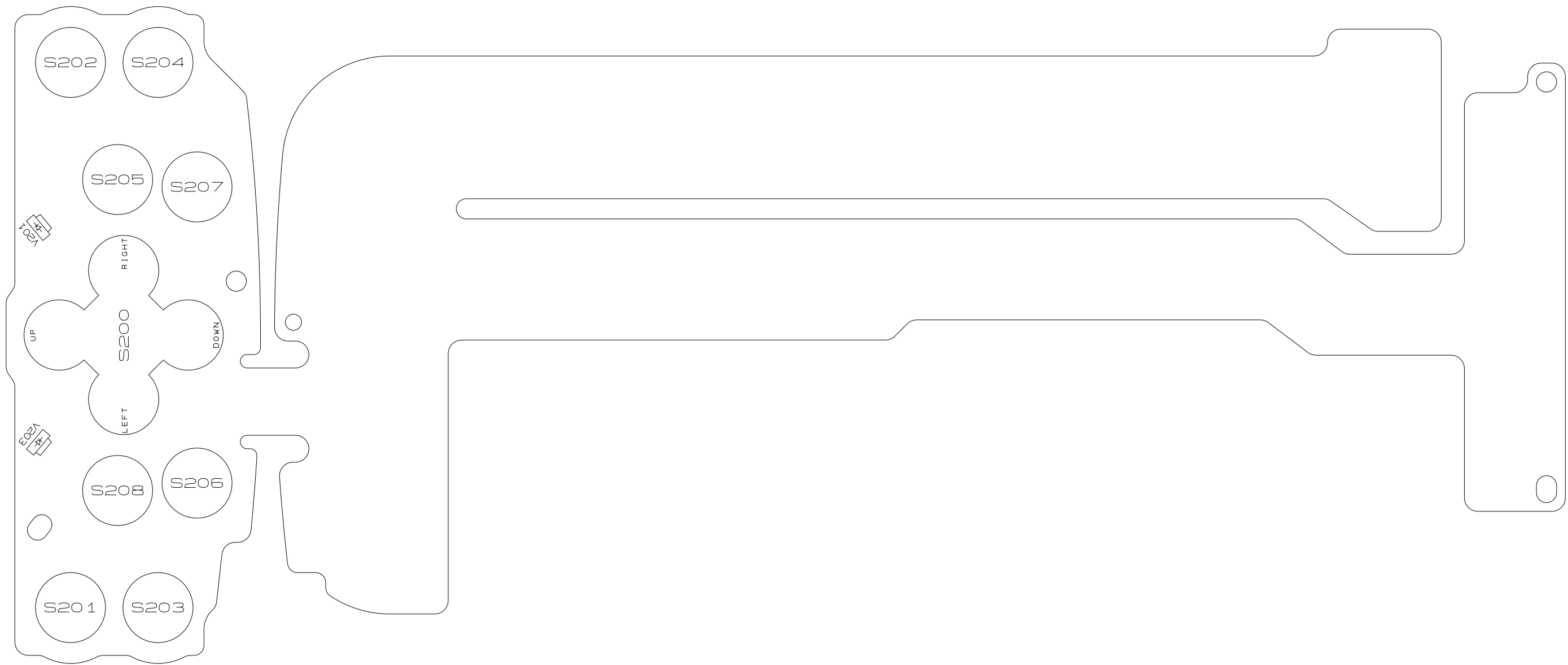




BB5.0 have defined 7-pin test pad pattern

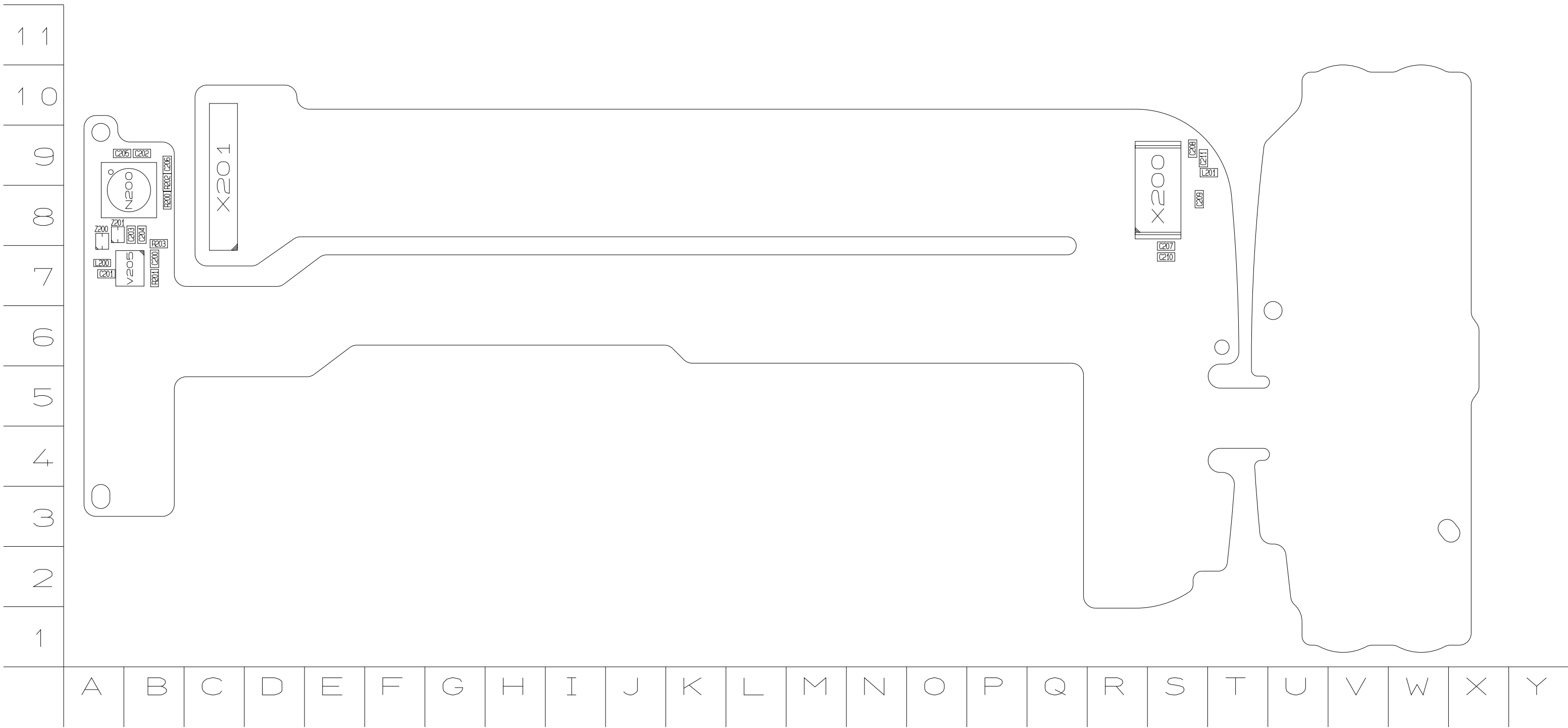


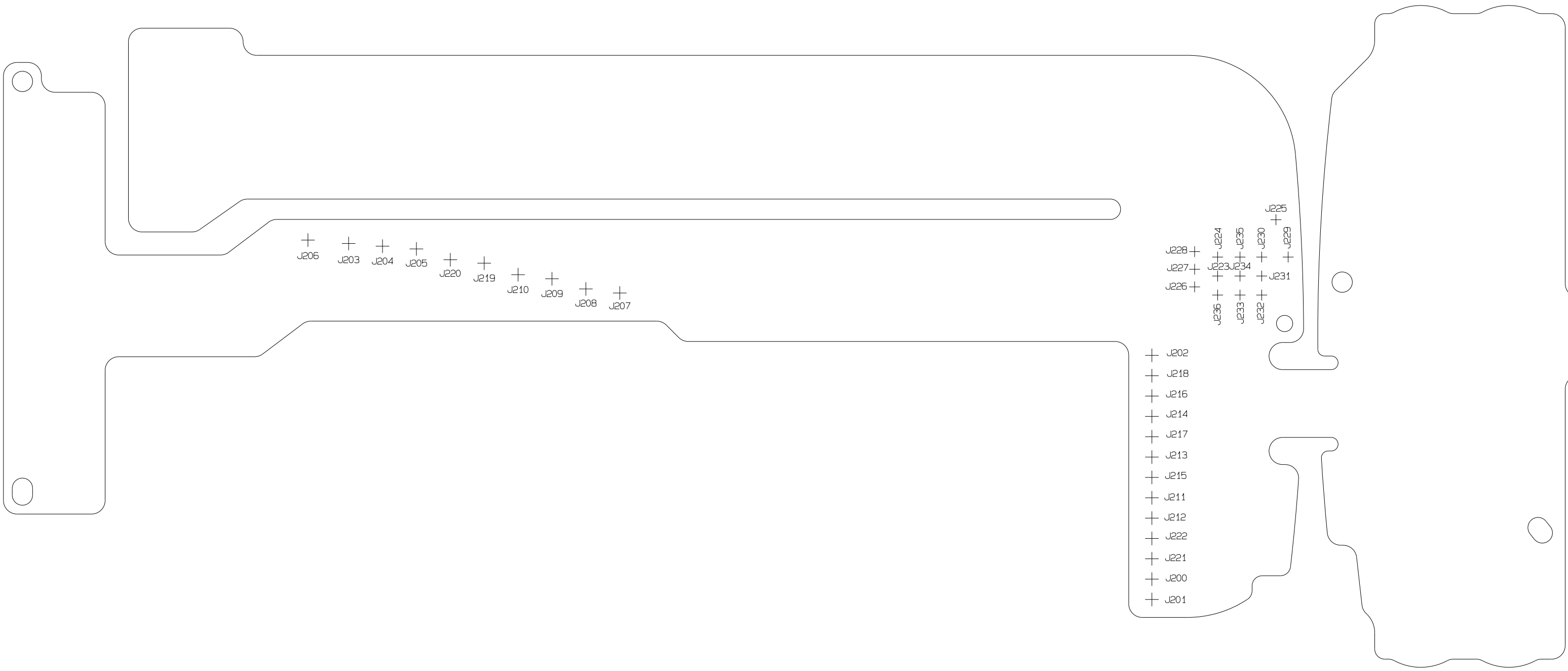




1	1
1	0
9	
8	
7	
6	
5	
4	
3	0
2	
1	

Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
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+ J206
+ J203
+ J204
+ J205
+ J220
+ J219
+ J210
+ J209
+ J208
+ J207

+ J202
+ J218
+ J216
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+ J231
+ J225

